CCD220 Back Illuminated L3Vision™ Sensor
Electron Multiplying Adaptive Optics CCD

FEATURES

- 240 x 240 pixel image area
- 24 µm square pixels
- Split frame transfer
- 100% fill factor
- Back-illuminated for high spectral response
- Metal-buttressed image and store clocks for high frame rates (1 kHz nominal)
- 8 L3Vision™ serial registers and very low noise outputs
- Integral compact Peltier package
- Deep depleted for red/NIR sensitivity

INTRODUCTION

The CCD220 is an L3Vision™ sensor designed for very high frame rate and low signal applications such as wavefront sensing or adaptive optics.

The image area is split into two half sections for split frame transfer operation using metal-buttressed electrodes for high speed. The image section can be operated in inverted mode if desired.

The device uses eight output amplifier circuits that are capable of operating at an equivalent output noise of less than one electron (rms) at frame rates of >1.2 kHz. All outputs must be used for full image read-out.

The Teledyne e2v back-thinning process ensures high quantum efficiency over a wide range of wavelengths, with a >90% typical peak response.

The device functions by converting photons to charge in the image area during the integration time period, then transferring this charge through one of the image and store sections into the readout register. Following transfer through the readout register, the charge is multiplied in the gain register prior to conversion to a voltage at the output amplifier. The multiplication gain may be varied by adjustment of the multiplication phase clock amplitude RØ2HV.

The device is supplied in a sealed integral Peltier package, which provides a nominal operating chip temperature of 233 K (-40 °C).

A variant of this device is also available with an integral shutter (CCD219).

Consult Teledyne e2v for further information.

TYPICAL PERFORMANCE

Readout frequency	13.6 MHz
Frame rate	1300 fps
Output responsivity	1.0 V/µe-
EM register gain	1000
Peak signal	300,000 e-/pixel
Readout noise	< 1 e- rms

GENERAL DATA

Device Format

Image area	5.76 x 5.76 mm
Image section active pixels	240 (H) x 240 (V)
Image pixel size	24 x 24 µm
Additional transition rows	2
Number of output amplifiers	8
Fill factor	100 %

Package (Nominal)

Package type	Compact Peltier package
Overall body dimensions	33.5 x 68.3 x 14.1 mm
Number of pins	64
Inter-pin spacing	1.778 mm
Opposite row spacing	33.53 mm
Temperature sensor	AD590KF
Window material	Sapphire
Package base operating temperature	10°C
Weight (approx.)	83 g

PART REFERENCE

CCD220-00-G-D36 G = Cosmetic Grade

Teledyne e2v (UK) Limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom Teledyne e2v (UK) Ltd. is a Teledyne Technologies company.
Telephone: +44 (0)1245 493493
Contact Teledyne e2v by e-mail: Enquiries@Teledyne-e2v.com or visit www.teledyne-e2v.com for global sales and operations centres.

A1A-781789 Version 4, February 2024

Approved for public release: Teledyne e2v APPROVED *(CM 5003115)*

TYPICAL PERFORMANCE SPECIFICATIONS

Except where otherwise specified, the following performances are applicable for operation at a pixel rate of 13.6 MHz and a frame rate of 1300 frames per second, with typical operating voltages. Parameters are given at the nominal operating temperature of -40°C (233 K).

Parameter	Min	Typical	Max	Units	Notes
Parallel transfer frequency	-	10	-	MHz	1
Readout frequency (settling to 1%) (Not Tested)	-	13.6	15	MHz	-
Parallel charge transfer efficiency	99.99	99.995	100	%	-
Serial charge transfer efficiency	99.95	99.985	100	%	2
Multiplication register gain	1	-	1000	-	3
Output amplifier responsivity	-	1	-	µV/e-	-
Image area peak charge storage	200,000	300,000	-	e-/px	-
Dark signal	-	0.005	0.015	e-/px/frame	-
Dark signal at 25 fps	-	0.1	0.4	e-/px/frame	-
Non-linearity (high gain mode)	-	-	3.5	%	4
Non-linearity (no gain)	-	-	2	%	5
Readout noise (high gain mode)	-	< 1	1	e- rms	6
Readout noise at 25 fps (high gain mode)	-	< 1	1	e- rms	6
Excess noise factor	-	√2	-	-	7
Amplifier reset noise (without CDS)	-	125	-	e- rms	-

NOTES

1. See drive pulse specifications and notes.
2. Specification applies for output signals <100,000 e-and gain <1000.
3. Some increase of RØ2HV may be required throughout life to maintain gain performance. Adjustment of RØ2HV should be limited to the maximum specified under Operating Conditions.
4. For signals of 10 e- to 150 e- at gain x1000.
5. For signals of 15,000 e- to 200,000 e- at gain x1.
6. Noise equivalent signal: if multiplication gain >50 is applied then the equivalent noise on the output signal due to an amplifier readout noise of 50 e-rms is < 1 e- rms.
7. The excess noise factor is defined as the factor by which the multiplication process increases the shot noise on the image when multiplication gain is used.

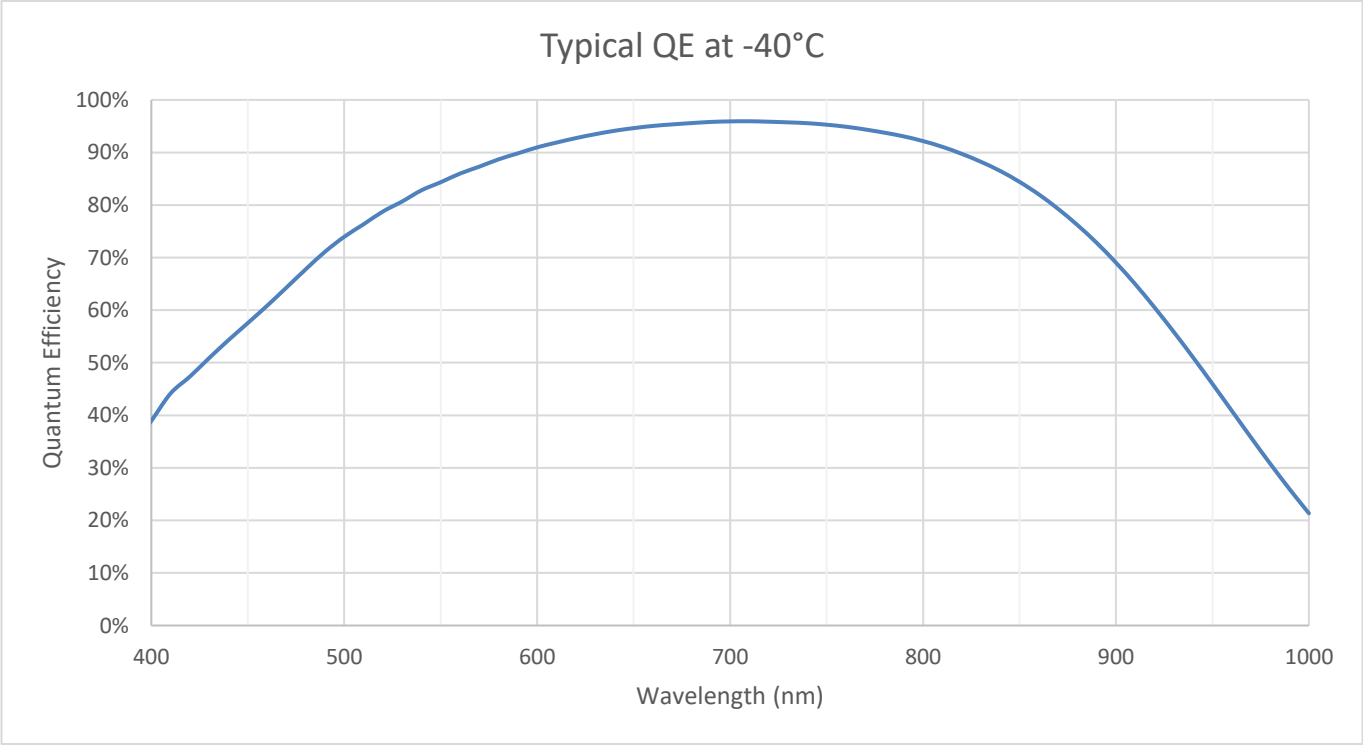
SPECTRAL RESPONSE

The table below gives the guaranteed minimum values of the spectral response for a deep depleted silicon device with an ER1 (extended red) anti-reflection coating at the test temperature of 20°C.

Wavelength (nm)	DD silicon ER1 AR Coating
	Minimum QE (%)
500	65
550	75
600	80
650	85
700	80
750	80
800	75
850	65
900	50

Spectral Response Graph

The spectral response graphs provided below are modelled values for a deep depleted silicon device with an ER1 (extended red) anti-reflection coating at the nominal operating temperature of -40°C (233K), and do not account for any transmission losses due to the package window. This data is theoretical and is not measured at the -40°C (233K) operating temperature.



BLEMISH SPECIFICATION

The table below gives defect specifications for a grade 1 device. Devices with lower cosmetic specifications (including mechanical samples) are subject to availability.

	Deep Depletion
Dark Pixels	≤ 10
Hot Pixels	≤ 10
Traps	≤ 10
Column Defects	0

Definitions

- A dark pixel is defined as a pixel which has less than 50% of the response of the mean, at a signal level corresponding to approximately half the full well capacity.
- A hot pixel is defined as a pixel which has a generation rate greater than 400 e-/px/s in darkness.
- A trap is a defect which can capture charge and release it in subsequent pixels, lines, or frames. A trap is defined as a defect with a capacity ≥ 5 e-.
- A column is counted as defective if it contains more than 5 contiguous dark pixels, hot pixels or traps.

PACKAGE SPECIFICATIONS

Parameter	Min	Typical	Max	Units	Notes
Flatness of image surface	-	-	20	µm	8
Optical distance from image plane to front of window	-	-	4	mm	-
Angle between image plane and front of window	-	-	3	deg (°)	-
Leak rate	-	-	$5x10^{-8}$	mbar l s^{-1}	9

Notes

8. ‘Peak to valley’ measurement.
9. Fine leak test detail only.

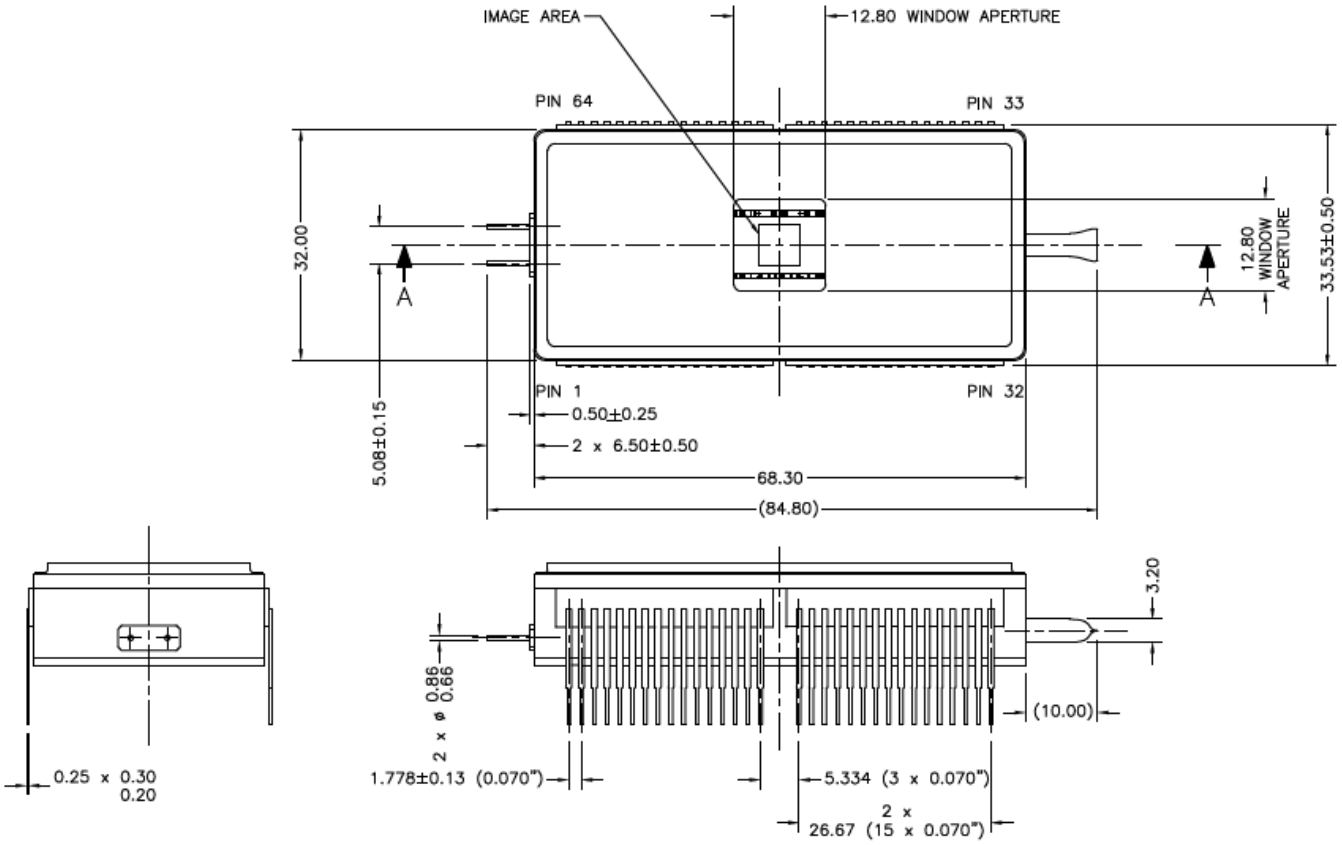
OPERATION OF PELTIER COOLER

Nominal operating details (steady state) for -40°C CCD operation with package coupled to a 10°C heat-sink are as follows:

Current (approx.) .....2.0 A
Voltage (approx.) ..... 5 V
Sensor dissipation .....< 2.5 W

Note that during cooling the Peltier cooler may draw in excess of 25 W. It is recommended that the cooling rate does not exceed 5°C per minute and, for optimum cooling, that the device remains unpowered until the operating temperature is reached. The positive peltier lead is the lead closest to pin 1.

PACKAGE DETAILS



Notes

10. The focal plane is 9.99 mm (nominal) above the package base.
11. Package height is 13.40 mm (nominal) from base to top of window.

ESD HANDLING PROCEDURES

CCD sensors, in common with most high performance IC devices, are sensitive to static electricity. In certain cases a static electricity discharge may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench.
- Operator wearing a grounded wrist strap.
- All receiving socket pins to be positively grounded.
- Unattended CCDs should not be left out of their conducting foam or socket.

All devices are provided with internal protection circuits to most gate electrodes but not to the other pins.

Evidence of incorrect handling will terminate the warranty.

OVERLOAD PRECAUTION

These devices can suffer reduced gain (ageing) if operated at high gain with high light levels. When operating with multiplication gain greater than unity it is recommended to keep signal levels below 100,000 e- at the output to avoid this effect.

MAXIMUM VOLTAGES BETWEEN PAIRS OF PINS

Pin	Connection	Pin	Connection	Min (V)	Max (V)
4	OS 7	3	OD 7	-15	+15
6	OS 8	7	OD 8	-15	+15
27	OS 4	26	OD 4	-15	+15
29	OS 3	30	OD 3	-15	+15
36	OS 2	35	OD 2	-15	+15
38	OS 1	39	OD 1	-15	+15
59	OS 5	58	OD 5	-15	+15
61	OS 6	62	OD 6	-15	+15
9	RØ2HV 7-8	8	RØDC 7-8	-20	+50
9	RØ2HV 7-8	54	RØ3 5-8	-20	+50
24	RØ2HV 3-4	25	RØDC 3-4	-20	+50
24	RØ2HV 3-4	43	RØ3 1-4	-20	+50
41	RØ2HV 1-2	40	RØDC 1-2	-20	+50
41	RØ2HV 1-2	43	RØ3 1-4	-20	+50
56	RØ2HV 5-6	57	RØDC 5-6	-20	+50
56	RØ2HV 5-6	54	RØ3 5-8	-20	+50

Notes

12. The package pin drawing is given on page 14.

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are with respect to substrate, SS.

Pin	Connection	Output Numbers	Min (V)	Max (V)
1	TS1 (+)	(See note 13)	-20	+44
2	RD	5-8	-0.3	+25
3	OD	7	-0.3	+32
4	OS	7 (See note 15)	-0.3	+25
5	SS	-	-	
6	OS	8 (See note 15)	-0.3	+25
7	OD	8	-0.3	+32
8	RØDC	7-8	-16	+16
9	RØ2HV	7-8	-16	+50
10	SS	-	-	
11	ØR	5-8	-16	+16
12	ØC	5-8	-16	+16
13	SS	-	-	
14	SØ1	5-8	-16	+16
15	SS	-	-	
16	IØ1	5-8	-16	+16
17	IØ1	1-4	-16	+16
18	SS	-	-	
19	SØ1	1-4	-16	+16
20	SS	-	-	
21	ØC	1-4	-16	+16
22	ØR	1-4	-16	+16
23	SS	-	-	
24	RØ2HV	3-4	-16	+50
25	RØDC	3-4	-16	+16
26	OD	4	-0.3	+32
27	OS	4 (See note 15)	-0.3	+25
28	SS	-	-	
29	OS	3 (See note 15)	-0.3	+25
30	OD	3	-0.3	+32
31	RD	1-4	-0.3	+25
32	Reserved	(See note 14)	-	

Pin	Connection	Output Numbers	Min (V)	Max (V)
33	Reserved	(See note 14)	-	
34	OG	1-4	-16	+16
35	OD	2	-0.3	+32
36	OS	2 (See note 15)	-0.3	+25
37	SS	-	-	
38	OS	1 (See note 15)	-0.3	+25
39	OD	1	-0.3	+32
40	RØDC	1-2	-16	+16
41	RØ2HV	1-2	-16	+50
42	SS	-	-	
43	RØ3	1-4	-16	+16
44	RØ2	1-4	-16	+16
45	RØ1	1-4	-16	+16
46	SØ2	1-4	-16	+16
47	SS	-	-	
48	IØ2	1-4	-16	+16
49	IØ2	5-8	-16	+16
50	SS	-	-	
51	SØ2	5-8	-16	+16
52	RØ1	5-8	-16	+16
53	RØ2	5-8	-16	+16
54	RØ3	5-8	-16	+16
55	SS	-	-	
56	RØ2HV	5-6	-16	+50
57	RØDC	5-6	-16	+16
58	OD	5	-0.3	+32
59	OS	5 (See note 15)	-0.3	+25
60	SS	-	-	
61	OS	6 (See note 15)	-0.3	+25
62	OD	6	-0.3	+32
63	OG	5-8	-16	+16
64	TS2 (-)	(See note 13)	0	-

Notes

13. An AD590KF temperature sensor is fitted.
14. Pins 32 and 33 are not connected, but reserved for other device variants.
15. Permanent damage may result if OS experiences short-circuit conditions during operation.
16. Maximum output transistor current = 20 mA.

OPERATING CONDITIONS

Typical operating voltages are as given in the table below. Some adjustment within the minimum-maximum range specified may be required to optimise performance. Operating voltages are with respect to ground.

Connection	Description	Pulse Amplitude or DC Level (V)		
		Min	Typical	Max
IØ1,2 high	Image Clocks (high) (see note 17)	-3	+3	+7
IØ1,2 low	Image Clocks (low)	-	-5	-
SØ1,2 high	Store Clocks (high)	-3	+3	+7
SØ1,2 low	Store Clocks (low)	-	-5	-
RØ1,2,3 high	Register Clocks (high)	+8	+12	+15
RØ1,2,3 low	Register Clocks (low)	-	0	-
RØ2HV high	Multiplication Register Clock (high)	+20	+45	+50
RØ2HV low	Multiplication Register Clock (low)	-2	+4	+5
ØR high	Reset Pulse (high)	+8	+10	+12
ØR low	Reset Pulse (low)	-	0	-
ØC high	DC Restore Clamp Pulse (high)	+8	+10	+12
ØC low	DC Restore Clamp Pulse (low)	-	0	-
RØDC	Multiplication Register DC Bias	0	+3.5	+6
OG	Output Gate	+1	+3	+5
OD	Output Drain	+24	+28	+32
RD	Reset Drain	+15	+17	+20
SS	Substrate	0	+3.5	+7

Notes

17. The image clock high level may need to be more positive than the minimum necessary for transfer in order to improve the point spread function. This can be achieved by increasing IØ high. Alternatively to ensure that clock-induced charge is kept to a minimum, three clock levels can be employed, integrating with an IØ clock high level greater than is used for transfer to the store region.
18. An external load is required for each output amplifier. The load should be either a 7.5 mA constant-current type or a 3.3 kΩ resistor connected to ground. The on-chip amplifier power dissipation is approximately 50 mW per output circuit.

DRIVE PULSE WAVEFORM SPECIFICATION

The following are suggested pulse rise and fall times for operation at 1300 frames per second with pixel readout at 13.6 MHz.

Clock Pulse	Typical Rise Time (ns)	Typical Fall Time (ns)	Typical Pulse Overlap	Notes
IØ	20	20	at 50% points	19
SØ	20	20	at 50% points	19
RØ1	5	5	at 70% points	
RØ2	5	5	at 70% points	
RØ3	5	5	at 70% points	
RØ2HV	25	25	For conventional clocking	20
RØ2HV	sine	sine	Sinusoid -high on falling edge of RØ1	20

Notes

19. For the parallel clocks the nominal frequency of operation during frame transfer is 10 MHz. There is some internal slowing of the drive pulse edges that should be a maximum of 6 ns and hence is unlikely to limit parallel transfer. The maximum frequency is probably limited by the practical constraints of generating suitable waveforms. The maximum rise/fall time is about half the clock period less 6 ns.
20. RØ2HV can be operated with a conventional clock pulse or a sinusoidal clock. The requirement for successful clocking is that RØ2HV reaches its maximum amplitude before RØ1 goes low.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances are defined at mid clock levels (for each device half-section).

Connection	Capacitance to SS (pF)	Inter-phase Capacitances (pF)	Total Capacitance (pF)	Series Resistance (Ω)	Output Impedance (Ω)
IØ1	640	230	870	2	-
IØ2	640	230	870	2	-
SØ1	550	240	790	2	-
SØ2	550	240	790	2	-
RØ1	81	34	115	10	-
RØ2	34	9	43	10	-
RØ3	87	31	118	10	-
RØ2HV	50	57	107	5	-
ØR	28	-	28	-	-
ØC	28	-	28	-	-
Each Amplifier	-	-	-	-	~350

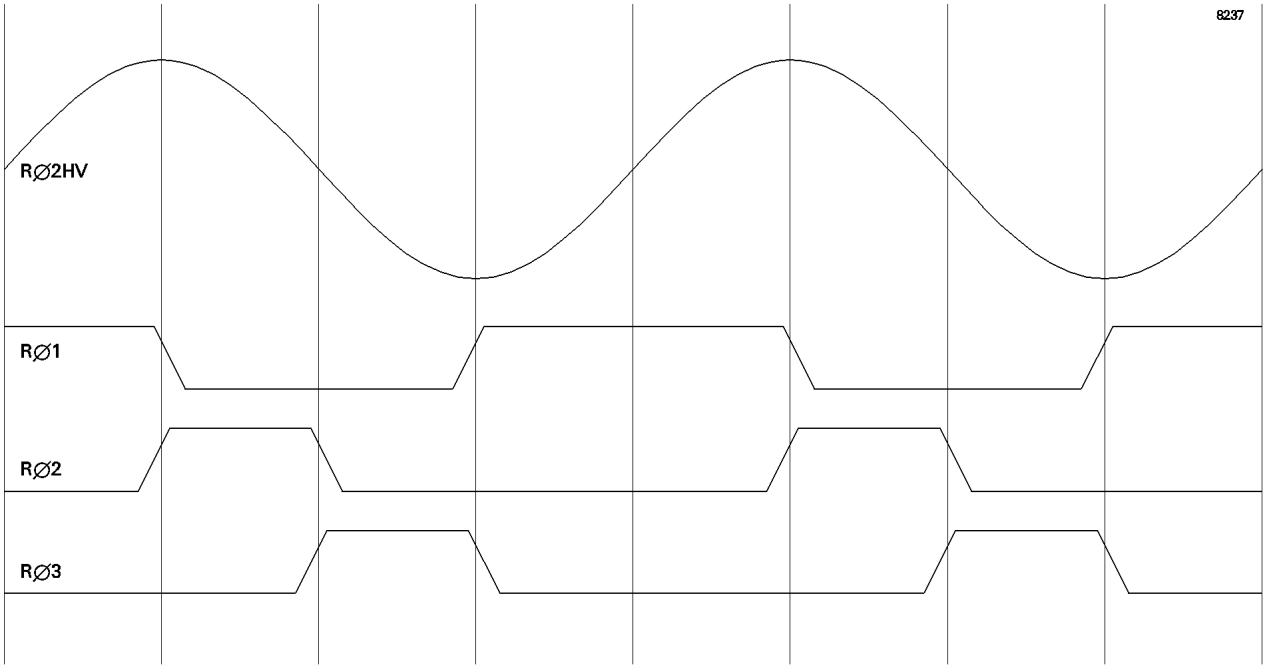
Notes

21. There will be some additional capacitance arising from the package, plus parasitic bond-wire and lead inductance of at least a few nH.

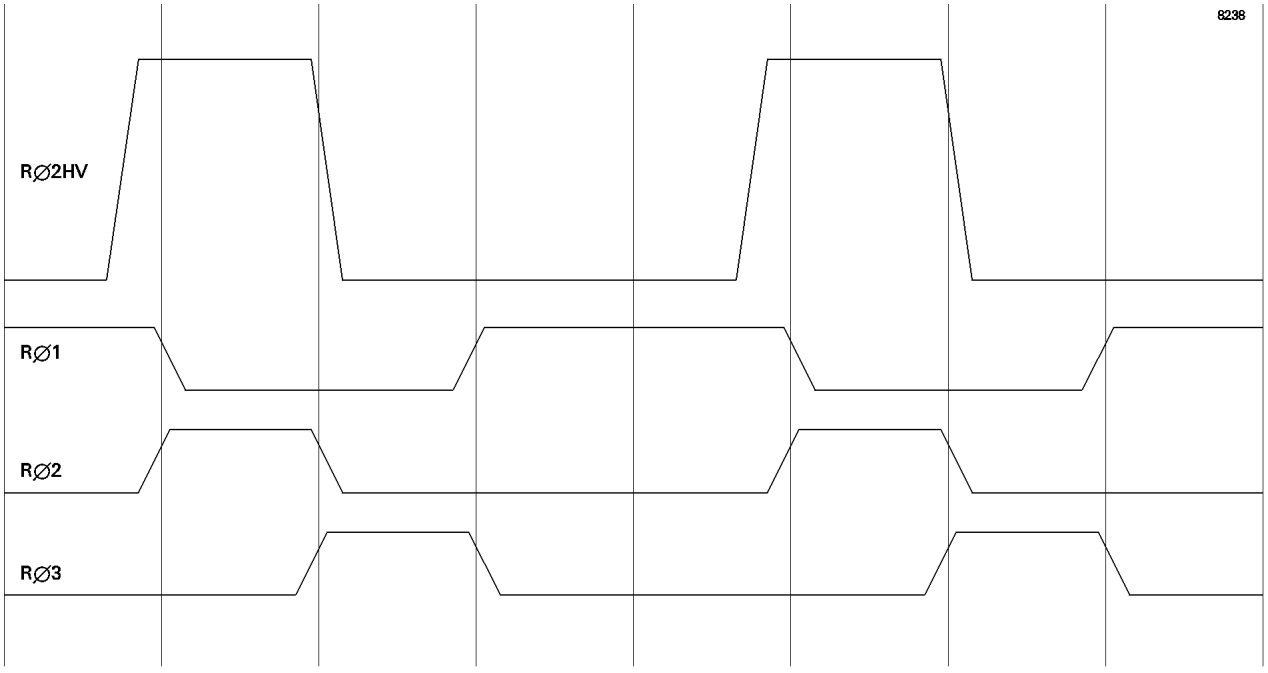
PULSE TIMINGS AND OVERLAPS

Clocking Scheme for Multiplication Gain

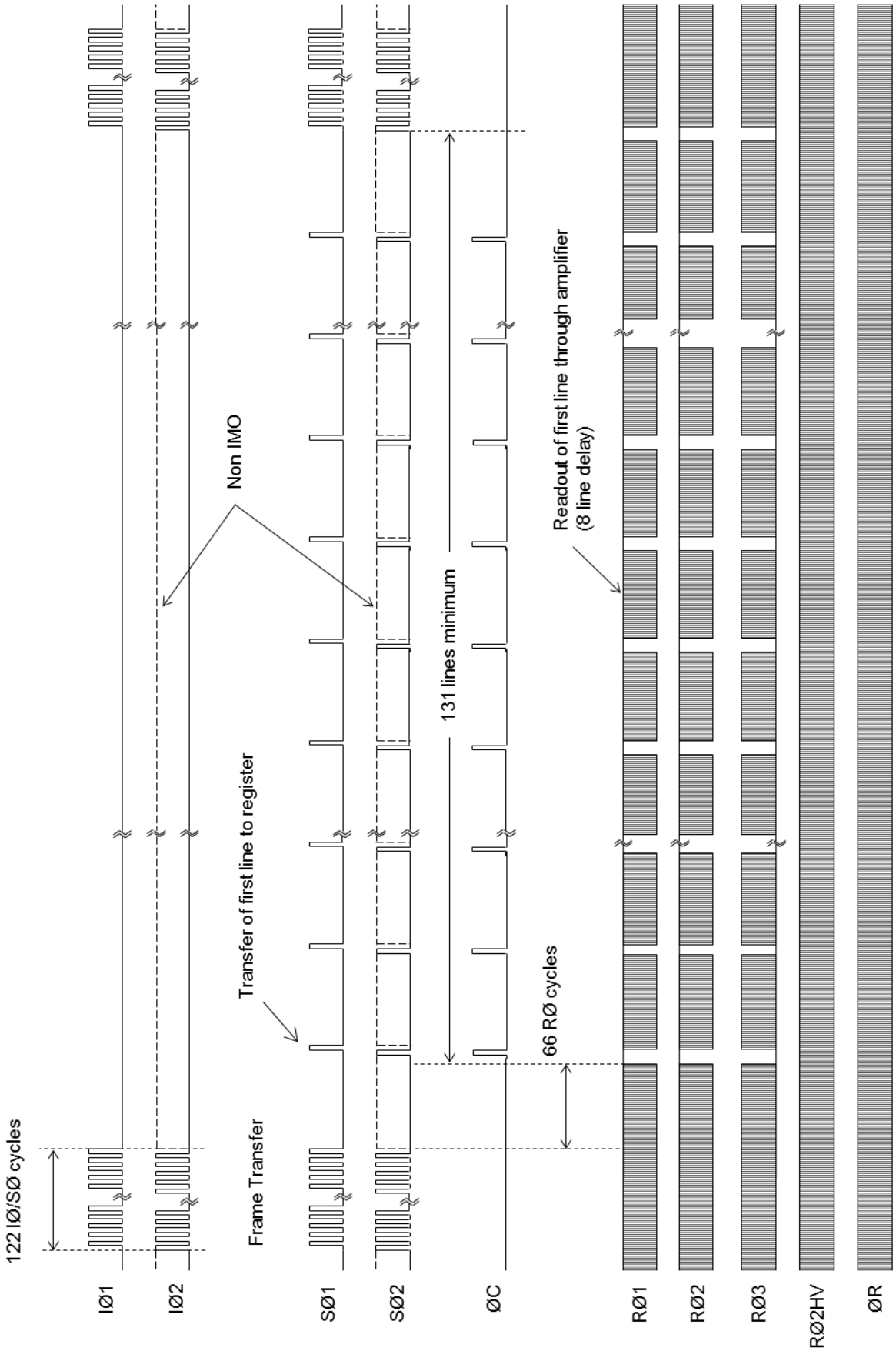
Sine wave clocking scheme:



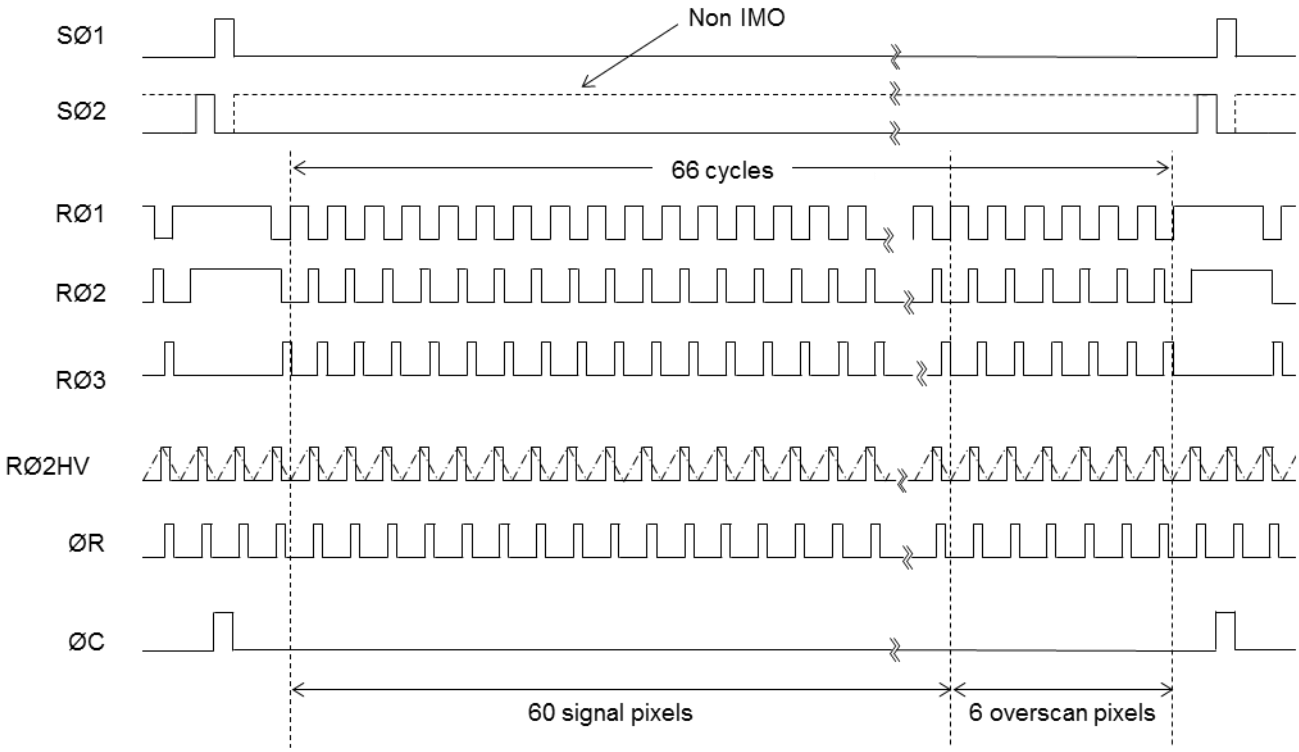
Conventional clocking scheme:



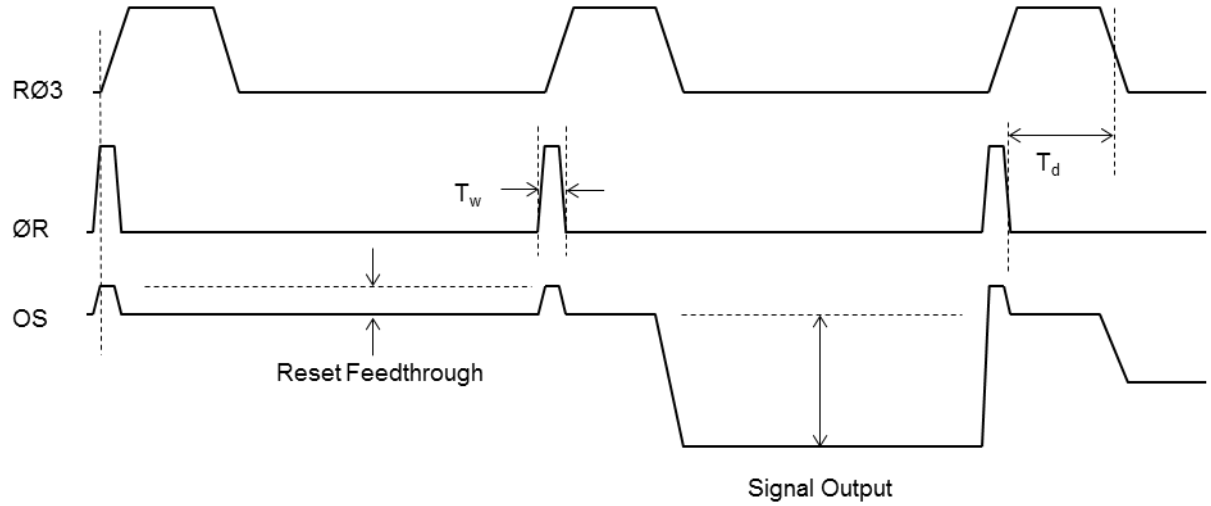
EXAMPLE FRAME TRANSFER TIMING DIAGRAM



EXAMPLE LINE TRANSFER TIMING DIAGRAM



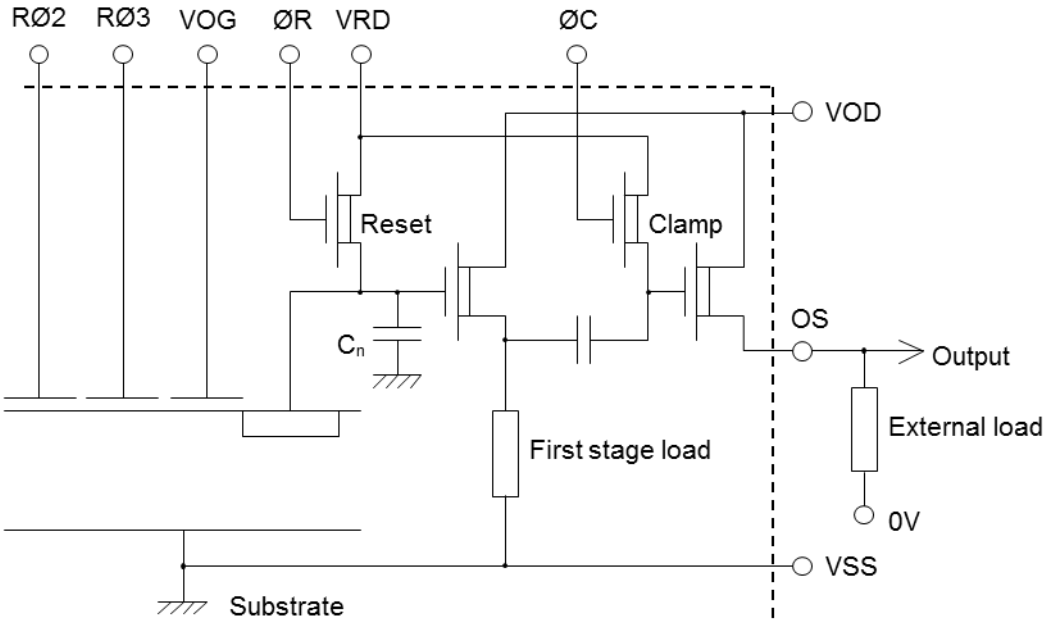
DETAIL OF OUTPUT TIMING



Notes

22. T_w = 10ns typical
23. T_d > 0 ns

OUTPUT CIRCUIT SCHEMATIC



SCHEMATIC CHIP DIAGRAM