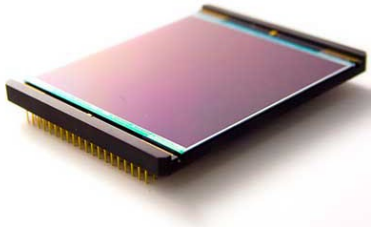
CCD231-84

16MP BSI CCD Sensor

(A) Buttable Package



(B) Ceramic PGA Package

KEY FEATURES

- Back Illuminated for high quantum efficiency
- Very Low readout noise
- 4 outputs
- Non-Inverted Mode Operation
- Deep depletion options for Red/NIR
- Uncoated option for soft X-Ray

TYPICAL APPLICATIONS

- Astronomy
- Scientific Imaging

OVERVIEW

The image area has four separately connected sections to allow full-frame, frame-transfer, split full-frame or split frame-transfer modes. Depending on the mode, the read out can be through 1, 2 or 4 of the output circuits. A gate-controlled drain is also provided adjacent to each of the registers to allow fast dumping of unwanted data.

The output amplifier is designed to give very low noise at read-out rates of up to 3 MHz. The low output impedance simplifies the interface with external electronics and the optional dummy outputs are provided to facilitate rejection of common parasitic feed-through.

A similar version (CCD230-84) is also available with higher charge handling capacity and higher speed (up to 5 MHz), but with slightly increased noise. These devices are inverted-mode operation.

GENERAL DATA

Format & Performance	
Image Area	61.4 x 61.7 mm
Active pixels	4096 (H) x 4112 (V)
Pixel Size	15 x 15 µm
Number of output amplifiers	4
Amplifier sensitivity	7.5 µV/e^-
Readout noise (rms)	5 e^- at 1 MHz 2 e^- at 50 kHz
Maximum pixel data rate	3 MHz
Peak Signal	350 ke^-/pixel
Flatness (both packages)	15 µm (peak to valley)
(A) Buttable Package	
Package size	63.0 x 69.0 mm
Package format	SiC & 2 flex connectors
Focal plane height, above base	15.0 mm
Height tolerance	±10 µm
Connectors	Two 37-way micro-D
(B) Ceramic-PGA Package	
Package size	63.8 x 79.6 mm
Package format	Aluminum Nitride PGA
Focal plane height, above base	3.6 mm
Connectors	Pin Grid Array (PGA)

PART REFERENCES

Please see last page for full list of available parts.

Custom options, such as alternative anti-reflection coatings or store shields, may be available upon request. Please contact Teledyne e2v for more details.

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A1A-765136 Version 11, July 2024
Template: 1B300000-DFP Ver 1
CM 5003532

Approved for public release: Teledyne e2v APPROVED

PERFORMANCE (at 173K unless stated)

Parameter		Grade 0 and 1			Grade 2			
		Typical	Min	Max	Min	Max	Units	Note
Peak charge storage (image)		350,000	275,000	-	250,000	-	e^-/pixel	2(a)
Peak charge storage (register/SW):	OG low (mode 1)	300,000	-	-	-	-	e^-/pixel	2(b)
	OG high (mode 2)	350,000	-	-	-	-	e^-/pixel	
Output node capacity:	OG low (mode 1)	250,000	-	-	-	-	e^-	2(c)
	OG high (mode 2)	600,000	-	-	-	-	e^-	
Output amplifier responsivity:	mode 1	7.5	5.0	-	4.5	-	µV/e^-	3
	mode 2	2.5	-	-	-	-	µV/e^-	
Readout noise		2	-	3	-	5	e^- rms	4
Readout frequency		500	-	3000	-	3000	kHz	5, 20
Dark signal:	At 173 K (measured)	3	-	100	-	364	e^-/pixel/hr	6
	At 153 K (calculated)	0.02	-	0.55	-	2.0	e^-/pixel/hr	
Charge transfer efficiency	Parallel	99.9995	99.9990	100	99.9985	100	%	7
	Serial	99.9995	99.9990	100	99.9985	100	%	
Flatness peak-to-valley		15	-	20	-	30	µm	8
Focal plane package height		15	14.990	15.010	14.985	15.015	mm	8, 9

NOTES

1. Device performance will be within the limits specified by “max” and “min” when operated at the recommended voltages supplied with the test data and when measured at a register clock frequency in the range 0.1 – 1.0 MHz. Most tests are performed at a nominal 500 kHz pixel rate. The noise as specified is separately measured in accordance with note 4.
2. (a) Signal level at which resolution begins to degrade. Device is non-inverted (NIMO/non-MPP), for maximum full well.

   (b) The summing well capacity limits the charge in the register, and its value varies with mode as shown.

   (c) The signal handled by the output node (for linear operation) varies with mode as shown. In mode 1 this is less than the typical pixel capacity and limits the dynamic range.
3. Under normal operation (mode 1), SW is operated as a summing well or clocked as R∅3. OG is biased at a low DC level. Note: in this mode (with lowest read noise) the output cannot handle the full available pixel charge capacity.

   Alternatively (mode 2), SW may be operated as an output gate (and not therefore available for summing), biased at a low DC level, with OG raised to a high voltage (see note 9). This gives more charge-handling capacity (e.g. for higher level pixel binning). Charge transfer to the output now occurs as R∅2 goes low. In mode-2, the output noise will also increase by a factor of three.
4. Measured with correlated double sampling at 50 kHz nominal (mode 1). Noise (as with all factory test images) is measured with differential readout, i.e. using the dummy output. The noise value reported is a single ended equivalent value with no dummy, by dividing by the √2 factor that arises from the differential subtraction. This way test system induced noise contribution is reduced.
5. Maximum frequency depends on the external load capacitance to be driven and the level of output settling required. Simulations show a settled waveform at 2 MHz with a 25 pF load, indicating that 3 MHz operation could be achievable with lower external loads. The register will transfer charge at higher frequencies, but performance cannot be guaranteed.

6. Dark signal is typically measured at a device temperature of 173 K. It is a strong function of temperature and the temperature dependence of dark signal at any temperature T (Kelvin) between 150 K and 300 K is given by:

   $Q_d/Q_{do} = 122T^3e^{-6400/T}$

   where Q_{do} is the dark current at 293 K. Typically Q_{do} is taken to have a value of 1 nA/cm^2, or ~14000 e-/pixel/s.

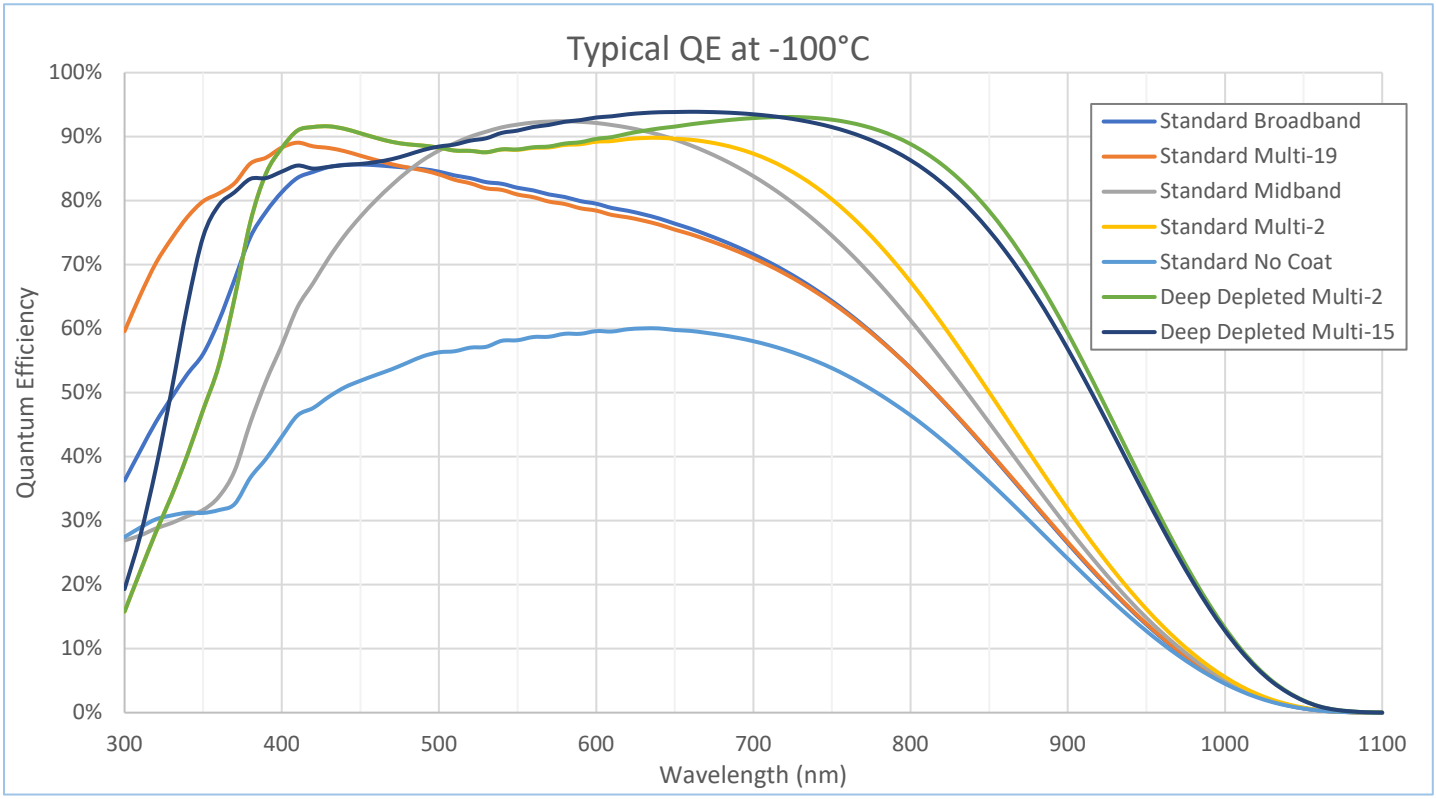
   Note that this typical value is based on a theoretical model and some variation may be seen between devices. Dark current is lowest with the substrate voltage at +9 V, and somewhat higher with substrate at 0 V. However, Vss=0V is recommended; see note 12 later. At cryogenic temperatures the dark current impact of low Vss is minor. Dark current can be reduced in operation by flushing the device whilst cooling and by setting VSS to +9V for a period before exposure. Longer periods of flushing will result in lower dark signal. Teledyne e2v do not optimise for ultimate dark signal performance during factory testing and reported values may be higher than the 3 e-/pixel/hr typical indicated at 173 K.

7. Measured with a ^{55}Fe X-ray source. The CTE value is quoted for the complete clock cycle (i.e. not per phase).
8. Mechanical parameters are measured at room temperature.
9. The package height measurement only applies to the buttable package option.

SPECTRAL RESPONSE

The table below gives guaranteed minimum values of the spectral response for several variants with enhanced BSI process. Photo response non-uniformity (PRNU) is also shown. See also the typical spectral response figures below.

Wavelength (nm)	Minimum Response (QE)							Max PRNU (1 σ)	
	Standard Silicon					Deep Depleted Silicon			
	Broadband	Multi-19	Midband	Multi-2	No Coat	Multi-2	Multi-15		
350	40	65	20	30	-	30	55	-	%
400	70	75	50	75	-	75	70	3	%
500	80	75	80	75	-	75	75	-	%
650	75	70	80	80	50	80	85	3	%
900	25	20	25	25	-	50	45	5	%



NOTES

10. The above specifications are for grade 0 and 1 devices. Grade 2 device specifications are 5% absolute lower for guaranteed QE minimum values and 1% absolute higher for guaranteed PRNU maximum values.
11. Standard silicon has a nominal active thickness of 16 µm. DD is Deep Depletion silicon with a higher resistivity and a nominal active thickness of 40 µm.
12. The availability of coatings varies depending on type; check with factory.
13. Devices with alternative or custom spectral response may be available by special request. Consult Teledyne e2v.
14. For No AR coat devices, PRNU is not measured nor guaranteed. Below approximately 200nm, the absorption length of incident photons in the AR coating material dominates and QE performance is lost. No AR coat devices are therefore desirable for the EUV or soft X-ray wavelength/energy range. In the visible range, they have lower performance than AR coated devices.

COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

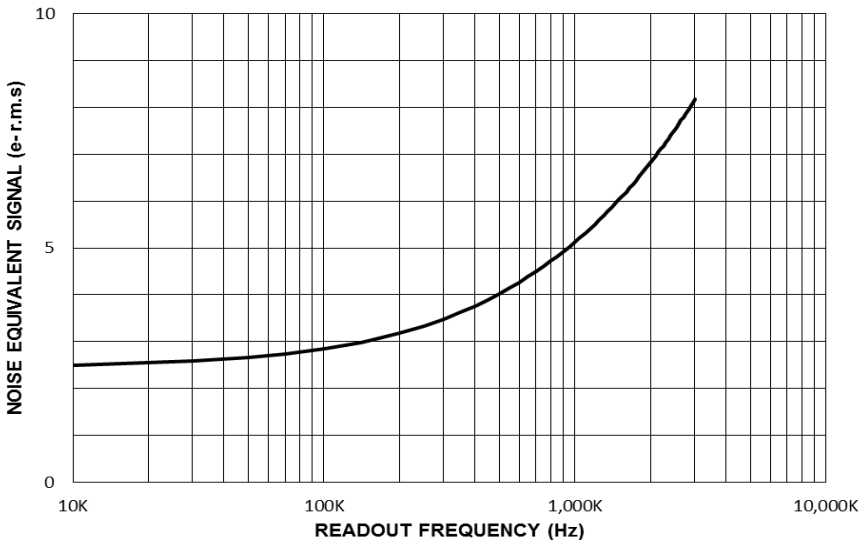
Standard and DD Silicon	Guaranteed Specifications			Typical Values		
Grade	0	1	2	0	1	2
Column defects - black or white	5	10	15	0	<3	<6
White spots	400	800	1200	<200	<400	<600
Total (black & white) spots	800	1500	2000	<400	<750	<1000
Traps > 200e-	10	15	20	<5	<10	<15

Cosmetic definitions

White spots	A defect is counted as a white spot if the dark generation rate is ≥5 e^-/pixel/s at 173 K. (which is also equivalent to ≥100 e^-/hour at 153 K). The temperature dependence is the same as for the mean dark signal; see note 6 above.
Black spots	A black spot defect is a pixel with a photo-response less than 50% of the local mean.
Column defects	A column is counted as a defect if it contains at least 100 white or dark single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel and released in to following pixels during readout. With the sensor uniformly illuminated to a signal level of approximately 1000e-, a column is counted as having a trap if the quantity of trapped charge released in to the overscan pixels is greater than 200 e^-.
Defect exclusion zone	Defect measurements are excluded from the outer two rows and columns of the sensor.

AMPLIFIER READ NOISE

The theoretical variation of typical read noise with operating frequency is shown below. (If measured using correlated double sampling with a pre-sampling bandwidth equal to twice the pixel rate in mode 1, temperature range 150 – 230 K).



DEFINITIONS

Back-thinning

A back-thinned CCD is fabricated on the front surface of the silicon and is subsequently processed for illumination from the reverse side. This avoids loss of transmission in the electrode layer (particularly significant at shorter wavelengths or with low energy X-rays). This process requires the silicon to be reduced to a thin layer by a combination of chemical and mechanical means. The surface is “passivated” and an anti-reflection coating may be added.

AR Coating

Anti-reflection coatings are normally applied to the back illuminated CCD to further improve the quantum efficiency. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For X-ray detection an uncoated device may be preferable.

Readout Noise

Readout noise is the random noise from the CCD output stage in the absence of signal. This noise introduces a random fluctuation in the output voltage that is superimposed on the detected signal.

The method of measurement involves reverse-clocking the register and determining the standard deviation of the output fluctuations, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dummy Output

Each output has an associated “dummy” circuit on-chip, which is of identical design to the “real” circuit but receives no signal charge. The dummy output should have the same levels of clock feed-through and can thus be used to suppress the similar component in the “real” signal output by means of a differential pre-amplifier. The penalty is that the noise is increased by a factor of $\sqrt{2}$. If not required, the dummy outputs may be powered down.

Dark Signal

This is the output signal of the device with zero illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration. Dark signal is a strong function of temperature as described in note 6.

Correlated Double Sampling

A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

Charge Transfer Efficiency

The fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature, and clock frequency.

ARCHITECTURE

Chip Schematic

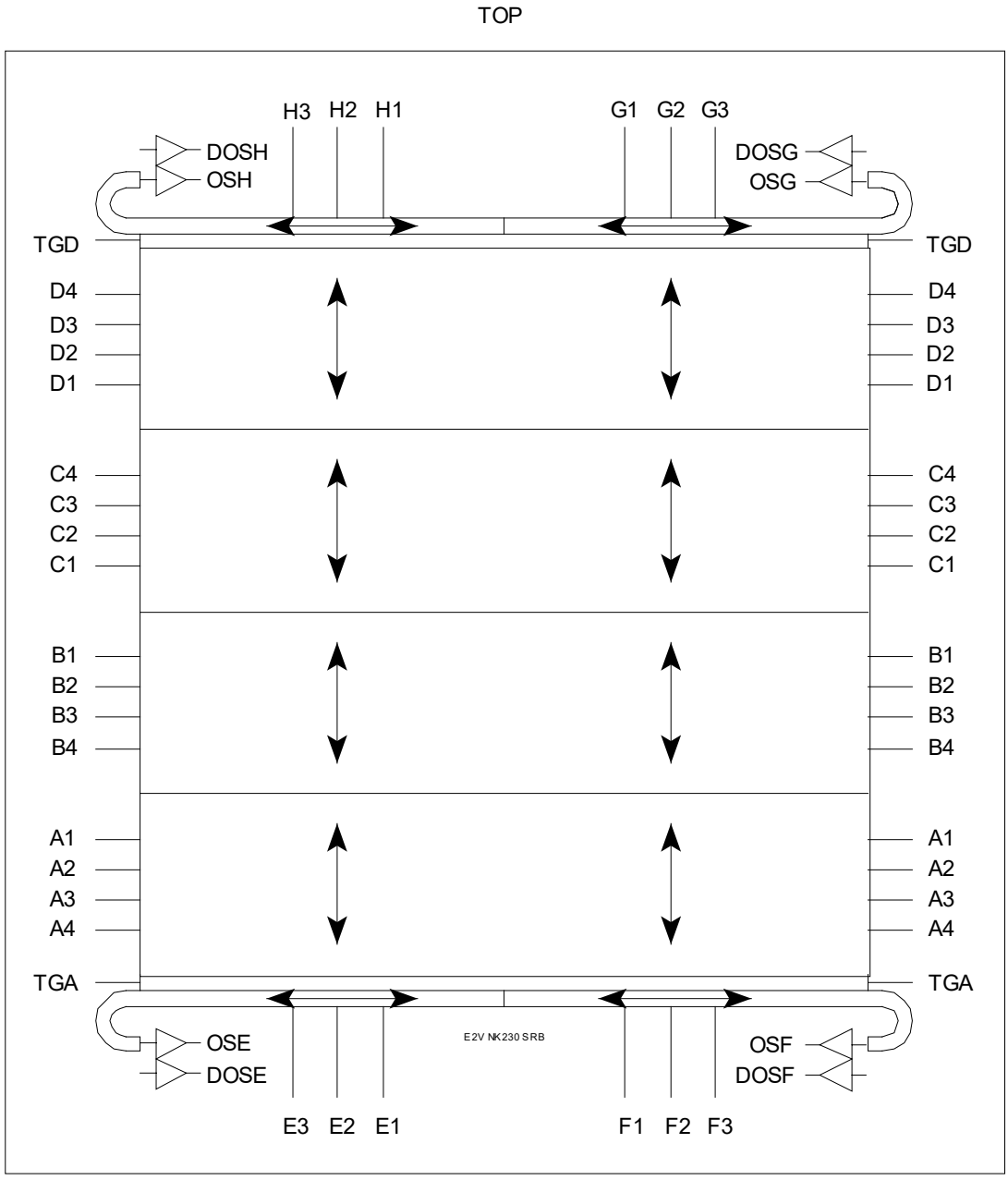
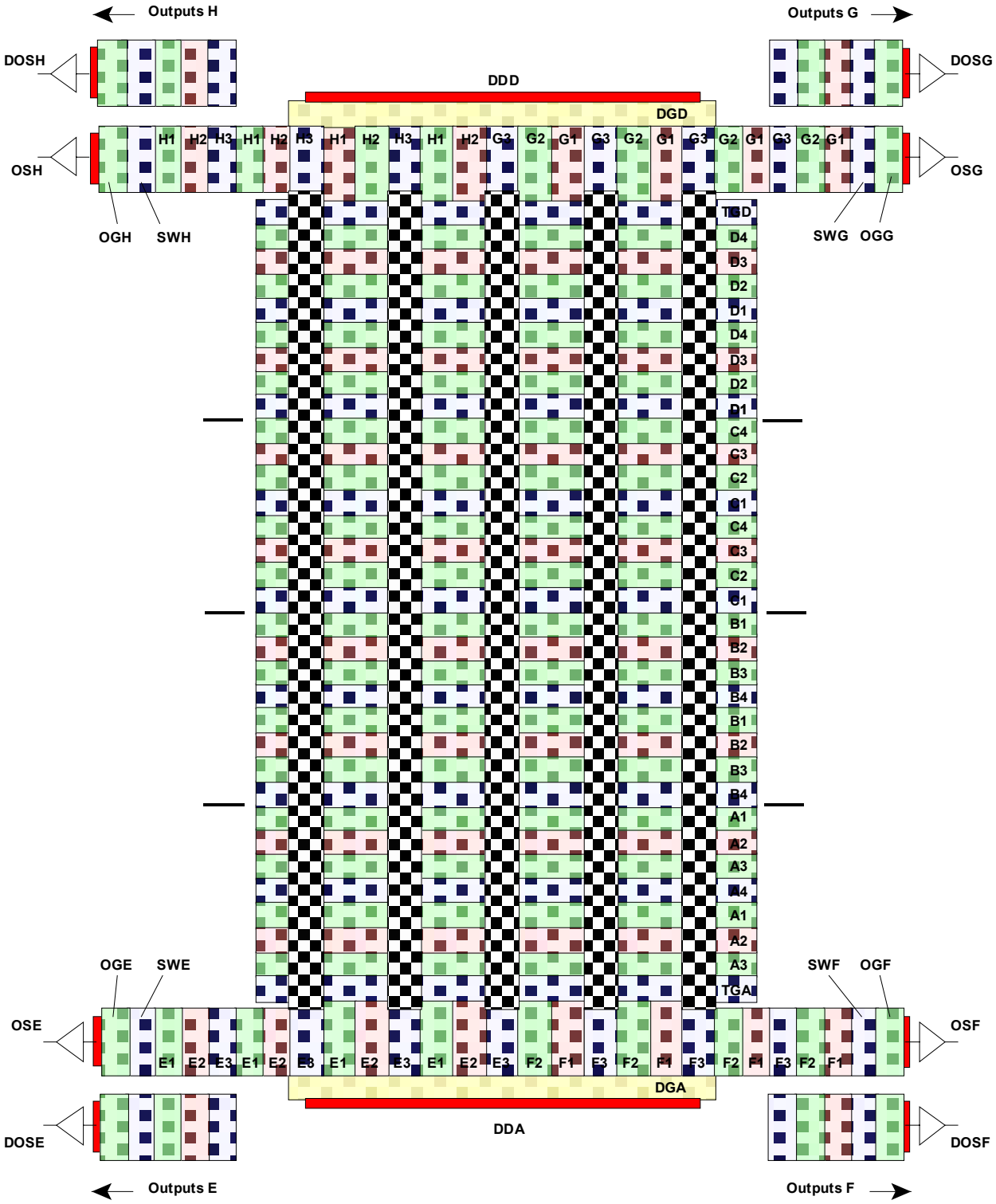


Image sections A and D each have a total of 4096 (H) x 1032 (V) pixels.

Image sections B and C each have a total of 4096 (H) x 1024 (V) pixels.

Connector-1 (and flexi) is at the “bottom” of the device (register E/F); Connector-2 is at the “top” of the device (register G/H).

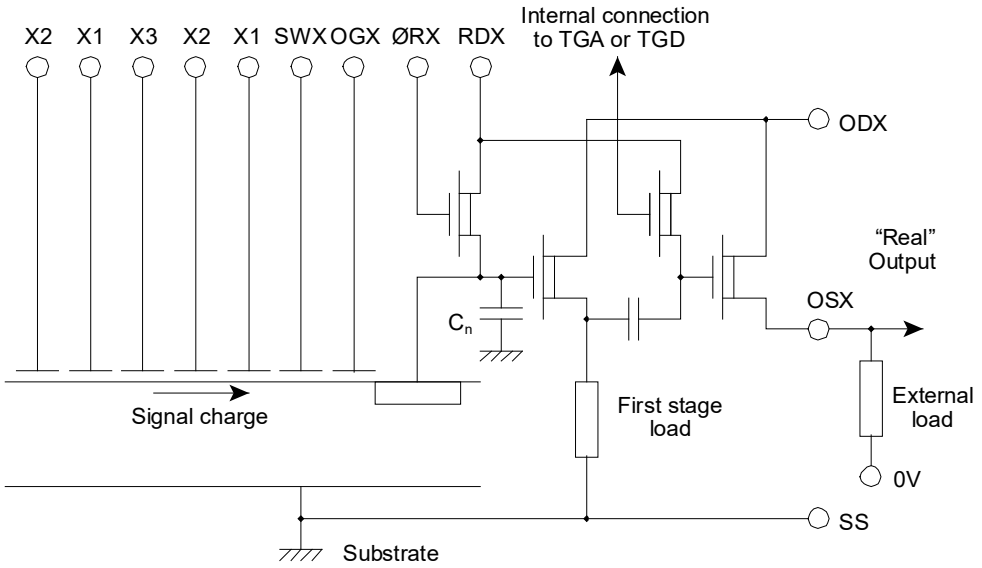
ARRANGEMENT OF ELECTRODES

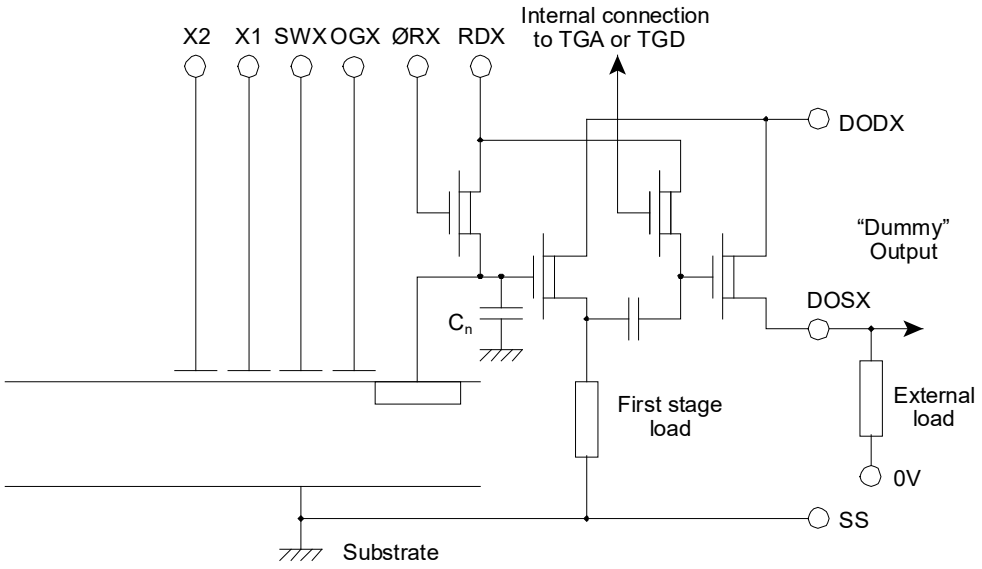


OUTPUT CIRCUIT

X designates a specific output, namely E, F, G or H .

The ‘mapping table’ on p18 shows the relationship between serial drive phases (R∅1, etc.) and device clock pins (X1, X2 etc)





The first stage load of each output (real or dummy) draws a quiescent current of approximately 0.2 mA via SS.

The output circuit consists of two capacitor-coupled source-follower stages. The particular design has a very high responsivity to give lowest noise. The load for the first stage is on-chip and that for the second stage is external, as next described. The DC restoration circuitry requires a pulse at the start of line readout, and this is automatically obtained by an internal connection to the adjacent transfer gate, TG. Transferring a line of charges to the register thus automatically activates the circuitry. N.B. TG pulses still need to be applied at similar intervals if only the register and/or output circuit are being operated, e.g. for test or characterisation purposes.

The amplifier output impedance is typically 400 Ω.

If an output is to be powered down, it is recommended that either OD or DOD be set to SS voltage, taking care that the maximum ratings are never exceeded. Alternatively, OD and DOD can be disconnected. If external loads return to a voltage below SS they should also be disconnected.

ELECTRICAL INTERFACE – A. Buttable package

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

Note that the hyphenated suffix symbols (e.g. ∅R-E) indicate to which output any register or amplifier pin relates.

Flex Connector 1

37W PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 17)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	SS	Substrate (see note 19)	0	0	10	N/A
2	DOS-E	Dummy Output Source (E)		(see note 15)		N/A
3	OS-E	Output Source (E)		(see note 15)		N/A
4	OG-E	Output Gate (E) (see note 16)	1	2.5	(note 16)	±20
5	DG-A	Dump Gate (A) (see note 18)	-2	0	0.5	±20
6	∅R-E	Reset Gate (E) (see note 20)	9	12	14	±20
7	SW∅-E	Summing Well (E) (see note 16)	9	10	12	±20
8	E1	Register Clock Phase 1 (E)	9	10	12	±20
9	E2	Register Clock Phase 2 (E)	9	10	12	±20
10	E3 – F3	Register Clock Phase 3 (E and F)	9	10	12	±20
11	F1	Register Clock Phase 1 (F)	9	10	12	±20
12	F2	Register Clock Phase 2 (F)	9	10	12	±20
13	SW∅-F	Summing Well (F) (see note 16)	9	10	12	±20
14	∅R-F	Reset Gate (F) (see note 20)	9	12	14	±20
15	TG-A	Transfer Gate (A)	9	10	12	±20
16	OG-F	Output Gate (F) (see note 16)	1	2.5	(note 16)	±20
17	OS-F	Output Source (F)		(see note 15)		N/A
18	DOS-F	Dummy Output Source (F)		(see note 15)		N/A
19	SS	Substrate (see note 20)	0	0	10	N/A
20	DOD-E	Dummy Output Drain (E)	27	29.5	33	–0.3 to +35
21	RD-E	Reset Drain (E)	16	17	19	–0.3 to +25
22	OD-E	Output Drain (E)	27	29.5	33	–0.3 to +35
23	SS	Substrate (see note 19)	0	0	10	N/A
24	A4	Image Area Clock Phase 4 (A)	9	10	12	±20
25	A3	Image Area Clock Phase 3 (A)	9	10	12	±20
26	B4	Image Area Clock Phase 4 (B)	9	10	12	±20
27	B3	Image Area Clock Phase 3 (B)	9	10	12	±20
28	SS	Substrate (see note 19)	0	0	10	N/A
29	DD-A	Dump Drain (A)	25	29	31	–0.3 to +35
30	B1	Image Area Clock Phase 1 (B)	9	10	12	±20
31	B2	Image Area Clock Phase 2 (B)	9	10	12	±20
32	A1	Image Area Clock Phase 1 (A)	9	10	12	±20
33	A2	Image Area Clock Phase 2 (A)	9	10	12	±20
34	SS	Substrate (see note 19)	0	0	10	N/A
35	OD-F	Output Drain (F)	27	29.5	33	–0.3 to +35
36	RD-F	Reset Drain (F)	16	17	19	–0.3 to +25
37	DOD-F	Dummy Output Drain (F)	27	29.5	33	–0.3 to +35

Flex Connector 2

37W PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 17)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	SS	Substrate (see note 19)	0	0	10	N/A
2	DOS-G	Dummy Output Source (G)		(see note 15)		N/A
3	OS-G	Output Source (G)		(see note 15)		N/A
4	OG-G	Output Gate (G) (see note 16)	1	2.5	(note 16)	±20
5	DG-D	Dump Gate (D) (see note 18)	-2	0	0.5	±20
6	∅R-G	Reset Gate (G) (see note 20)	9	12	14	±20
7	SW∅-G	Summing Well (G) (see note 16)	9	10	12	±20
8	G1	Register Clock Phase 1 (G)	9	10	12	±20
9	G2	Register Clock Phase 2 (G)	9	10	12	±20
10	G3 – H3	Register Clock Phase 3 (G and H)	9	10	12	±20
11	H1	Register Clock Phase 1 (H)	9	10	12	±20
12	H2	Register Clock Phase 2 (H)	9	10	12	±20
13	SW∅-H	Summing Well (H) (see note 16)	9	10	12	±20
14	∅R-H	Reset Gate (H) (see note 20)	9	12	14	±20
15	TG-D	Transfer Gate (D)	9	10	12	±20
16	OG-H	Output Gate (H) (see note 16)	1	2.5	(note 16)	±20
17	OS-H	Output Source (H)		(see note 15)		N/A
18	DOS-H	Dummy Output Source (H)		(see note 15)		N/A
19	SS	Substrate (see note 19)	0	0	10	N/A
20	DOD-G	Dummy Output Drain (G)	27	29.5	33	–0.3 to +35
21	RD-G	Reset Drain (G)	16	17	19	–0.3 to +25
22	OD-G	Output Drain (G)	27	29.5	33	–0.3 to +35
23	SS	Substrate (see note 19)	0	0	10	N/A
24	D1	Image Area Clock Phase 1 (D)	9	10	12	±20
25	D2	Image Area Clock Phase 2 (D)	9	10	12	±20
26	C1	Image Area Clock Phase 1 (C)	9	10	12	±20
27	C2	Image Area Clock Phase 2 (C)	9	10	12	±20
28	SS	Substrate (see note 19)	0	0	10	N/A
29	DD-D	Dump Drain (D)	25	29	31	–0.3 to +35
30	C4	Image Area Clock Phase 4 (C)	9	10	12	±20
31	C3	Image Area Clock Phase 3 (C)	9	10	12	±20
32	D4	Image Area Clock Phase 4 (D)	9	10	12	±20
33	D3	Image Area Clock Phase 3 (D)	9	10	12	±20
34	SS	Substrate (see note 20)	0	0	10	N/A
35	OD-H	Output Drain (H)	27	29.5	33	–0.3 to +35
36	RD-H	Reset Drain (H)	16	17	19	–0.3 to +25
37	DOD-H	Dummy Output Drain (H)	27	29.5	33	–0.3 to +35

Note that parallel clock phase designations (sequence of phases) differ for Connector 2 compared with Connector 1.

NOTES

15. Do not connect to voltage supply but use a ~5 mA current source or a ~5 kΩ external load. The quiescent voltage on OS is then about 6 - 8 V above the reset drain voltage and is typically 24 V. The current through these pins must not exceed 20 mA. Permanent damage may result if, in operation, OS or DOS experience short circuit conditions.

    For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz then the load may be increased to 10 kΩ to reduce power consumption.

16. Default operation (mode 1) shown with OG set to OG-Lo, with a +2.5 V nominal value. In this mode SW may be clocked as R∅3 if a summing well function is not required. OG-Lo should have a maximum value of +5 V.

    For alternative operation in a low responsivity mode (mode 2) with increased charge handling, OG should be set to OG-Hi and SW should be operated as OG-Lo (i.e. 2 V typical). See below for appropriate OG-Hi values. Charge is now read out as R∅2 goes low.

    See note 20 also for discussion about Substrate voltage (Vss). With high substrate voltage OG-Hi may be set to a nominal +20 V, which offers best linearity in mode-2. With low substrate voltage, the allowed maximum value of OG-Hi is limited to a nominal +18 V; the lower OG-Hi value has a greater non-linearity.

17. To ensure that any device can be operated the camera should be designed so that any value in the range “min” to “max” can be provided. All operating voltages are with respect to image clock low (nominally 0 V).

    The clock pulse low levels should be in the range 0 ± 0.5 V for image clocks. The register and SW clock low level should be +1 V higher. Reset clock low may be nominally 0 V or +1 V.

    In all cases, specific recommended settings will be supplied with each science-grade sensor.

18. Non-charge dumping level shown. For charge dumping, DG should be pulsed to 12 ± 2 V.

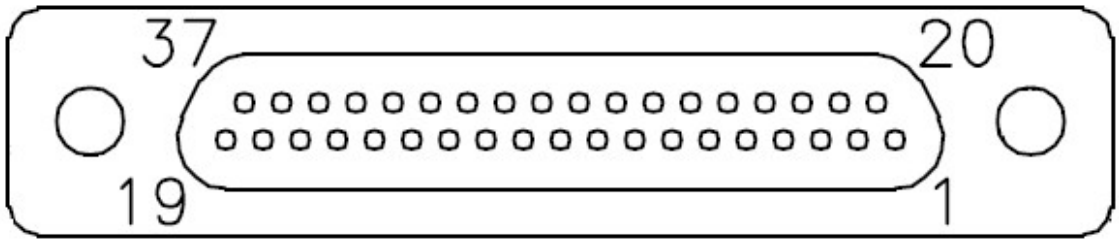
19. The substrate voltage (Vss) has a default recommended value of 0 V (“low” substrate). This is particularly recommended for deep-depletion device variants, since it optimises depletion depth for best Point Spread Function. Devices may alternatively be operated at “high” substrate, with Vss = 9 V. The high substrate setting offers slightly lower dark current, although this is usually not of primary concern when the device is cryogenically cooled.

    The substrate setting has some consequence for the allowed OG upper voltage level, as discussed in note 17.

20. Standard silicon variants are expected to be used with ∅R at +10 V or more; deep depletion variants require at least +12 V. A higher value will give a correspondingly higher reset feedthrough signal in the device output (OS).

This data sheet assumes that all signals are relative to the clock low level of 0V. The absolute level for all biases and clock rails may be changed to suit the needs of the designer provided the relative levels are maintained. For example, it is acceptable to change Vss so long as the specified difference between Vss and all other bias and clock voltages is maintained and the current load on all output sources is as recommended in note 16.

PIN CONNECTIONS (View facing pins of connector)



This numbering applies to all connectors. The connector is a Glenair 37P micro D type.

The CCD231-C6 has the same connections.

ELECTRICAL INTERFACE – B. Ceramic-PGA package

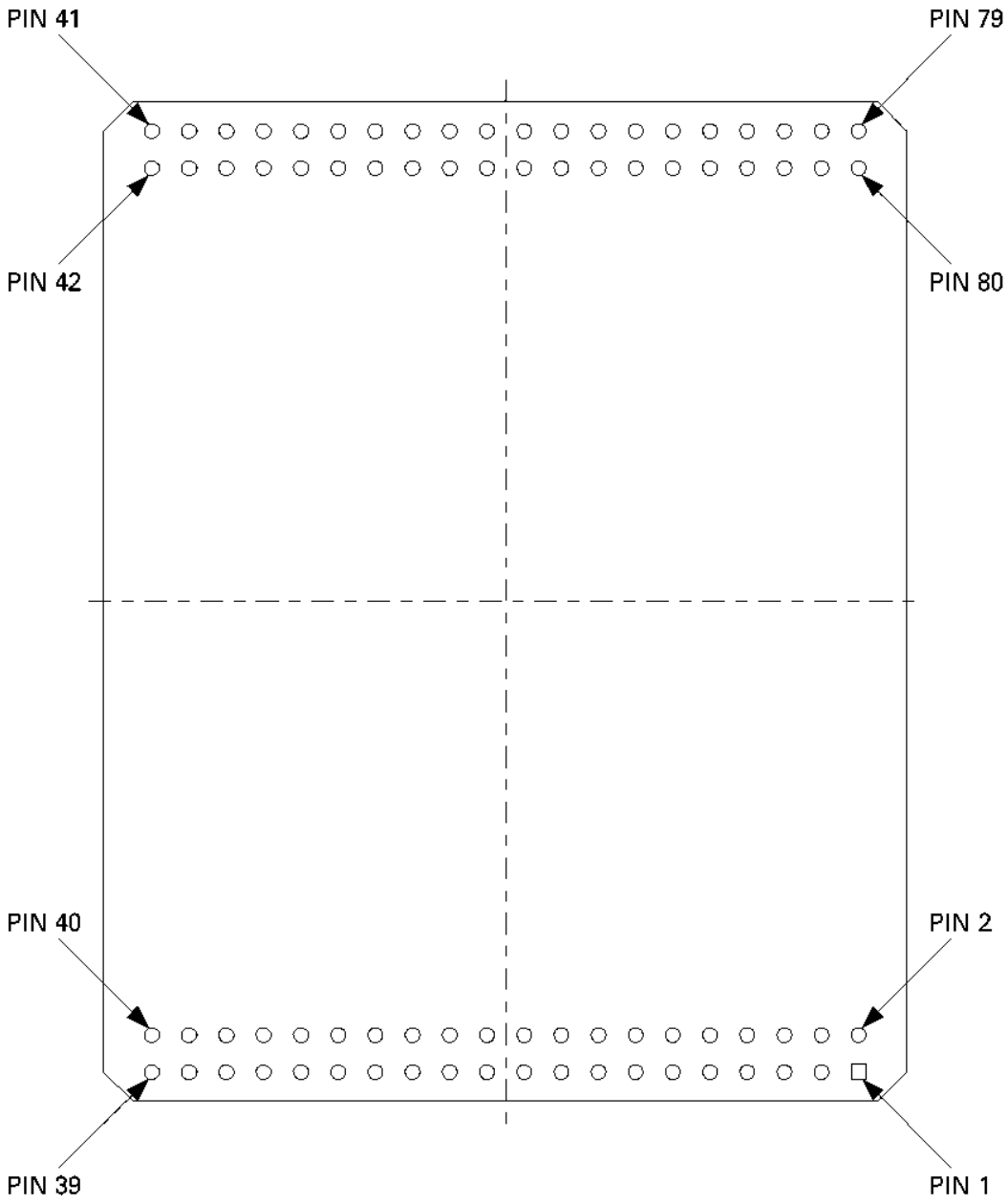
CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

The tables below give the pin-outs and clock amplitudes. Note that the hyphenated suffix symbols (e.g. ∅R-H) indicate to which amplifier the CCD pin relates.

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 17)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	DOS-E	Dummy Output Source (E)		(see note 15)		-0.3 to +25
2	DOD-E	Dummy Output Drain (E)	27	29.5	33	29
3	OS-E	Output Source (E)		(see note 15)		-0.3 to +25
4	OD-E	Output Drain (E)	27	29.5	33	-0.3 to +35
5	RD-E	Reset Drain (E)	16	17	19	-0.3 to +25
6	SS	Substrate (see note 19)	0	0	10	N/A
7	OG-E	Output Gate (E) (see note 16)	1	2.5	(note 16)	±20
8	SW∅-E	Summing Well (E) (see note 16)	9	10	12	±20
9	E3	Register Clock Phase 3 (E)	9	10	12	±20
10	∅R-E	Reset Gate (E) (see note 20)	9	12	14	±20
11	E2	Register Clock Phase 2 (E)	9	10	12	±20
12	E1	Register Clock Phase 1 (E)	9	10	12	±20
13	A1	Image Area Clock Phase 1 (A)	9	10	12	±20
14	SS	Substrate (see note 19)	0	0	10	N/A
15	A2	Image Area Clock Phase 2 (A)	9	10	12	±20
16	A3	Image Area Clock Phase 3 (A)	9	10	12	±20
17	SS	Substrate (see note 19)	0	0	10	N/A
18	A4	Image Area Clock Phase 4 (A)	9	10	12	±20
19	TS-1	Temperature Sensor 1 – Pin 1		(see note 26)		N/A
20	DG-A	Dump Gate (A) (see note 17)	-2	0	0.5	±20
21	TS-2	Temperature Sensor 1 – Pin 2		(see note 26)		N/A
22	DD-A	Dump Drain (A)	25	29	31	-0.3 to +35
23	TG-A	Transfer Gate (A)	9	10	12	±20
24	B4	Image Area Clock Phase 4 (B)	9	10	12	±20
25	B2	Image Area Clock Phase 2 (B)	9	10	12	±20
26	B3	Image Area Clock Phase 3 (B)	9	10	12	±20
27	B1	Image Area Clock Phase 1 (B)	9	10	12	±20
28	SS	Substrate (see note 19)	0	0	10	N/A
29	F1	Register Clock Phase 1 (F)	9	10	12	±20
30	F2	Register Clock Phase 2 (F)	9	10	12	±20
31	F3	Register Clock Phase 3 (F)	9	10	12	±20
32	∅R-F	Reset Gate (F) (see note 20)	9	12	14	±20
33	OG-F	Output Gate (F) (see note 16)	1	2.5	(note 16)	±20
34	SW∅-F	Summing Well (F) (see note 16)	9	10	12	±20
35	RD-F	Reset Drain (F)	16	17	19	-0.3 to +25
36	SS	Substrate (see note 19)	0	0	10	N/A
37	OS-F	Output Source (F)		(see note 15)		-0.3 to +25
38	OD-F	Output Drain (F)	27	29.5	33	-0.3 to +35
39	DOS-F	Dummy Output Source (F)		(see note 15)		-0.3 to +25
40	DOD-F	Dummy Output Drain (F)	27	29.5	33	-0.3 to +35

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 17)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
41	DOS-G	Dummy Output Source (G)		(see note 15)		-0.3 to +25
42	DOD-G	Dummy Output Drain (G)	27	29.5	33	29
43	OS-G	Output Source (G)		(see note 15)		-0.3 to +25
44	OD-G	Output Drain (G)	27	29.5	33	-0.3 to +35
45	RD-G	Reset Drain (G)	16	17	19	-0.3 to +25
46	SS	Substrate (see note 19)	0	0	10	N/A
47	OG-G	Output Gate (G) (see note 16)	1	2.5	(note 16)	±20
48	SW∅-G	Summing Well (G) (see note 16)	9	10	12	±20
49	G3	Register Clock Phase 3 (G)	9	10	12	±20
50	∅R-G	Reset Gate (G) (see note 20)	9	12	14	±20
51	G2	Register Clock Phase 2 (G)	9	10	12	±20
52	G1	Register Clock Phase 1 (G)	9	10	12	±20
53	D4	Image Area Clock Phase 4 (D)	9	10	12	±20
54	SS	Substrate (see note 19)	0	0	10	N/A
55	D3	Image Area Clock Phase 3 (D)	9	10	12	±20
56	D2	Image Area Clock Phase 2 (D)	9	10	12	±20
57	SS	Substrate (see note 19)	0	0	10	N/A
58	D1	Image Area Clock Phase 1 (D)	9	10	12	±20
59	TS-3	Temperature Sensor 2 – Pin 1		(see note 26 later)		N/A
60	DG-D	Dump Gate (D) (see note 18)	-2	0	0.5	±20
61	TS-4	Temperature Sensor 2 – Pin 2		(see note 26 later)		N/A
62	DD-D	Dump Drain (D)	25	29	31	-0.3 to +35
63	TG-D	Transfer Gate (D)	9	10	12	±20
64	C1	Image Area Clock Phase 1 (C)	9	10	12	±20
65	C3	Image Area Clock Phase 3 (C)	9	10	12	±20
66	C2	Image Area Clock Phase 2 (C)	9	10	12	±20
67	C4	Image Area Clock Phase 4 (C)	9	10	12	±20
68	SS	Substrate (see note 20)	0	0	10	N/A
69	H1	Register Clock Phase 1 (H)	9	10	12	±20
70	H2	Register Clock Phase 2 (H)	9	10	12	±20
71	H3	Register Clock Phase 3 (H)	9	10	12	±20
72	∅R-H	Reset Gate (H) (see note 20)	9	12	14	±20
73	OGH	Output Gate (H) (see note 16)	1	2.5	(note 16)	±20
74	SW∅-H	Summing Well (H) (see note 16)	9	10	12	±20
75	RD-H	Reset Drain (H)	16	17	19	-0.3 to +25
76	SS	Substrate (see note 19)	0	0	10	N/A
77	OS-H	Output Source (H)		(see note 15)		-0.3 to +25
78	OD-H	Output Drain (H)	27	29.5	33	-0.3 to +35
79	DOS-H	Dummy Output Source (H)		(see note 15)		-0.3 to +25
80	DOD-H	Dummy Output Drain (H)	27	29.5	33	-0.3 to +35

PIN CONNECTIONS (View facing underside of ceramic-PGA package)



ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (defined at mid-clock level)

	Typical	Units
I∅/I∅ inter-phase [A, B, C and D]	10	nF
I∅/SS [A, B, C and D)	20	nF
Transfer gates [TGA, TGD]	75	pF
R∅ total [E1, F1, G1, H1]	190	pF
R∅ total [E2, F2, G2, H2]	175	pF
R∅ total [E3, F3, G3, H3]	155	pF

The total capacitance on each phase is the sum of the inter-phase capacitance to each of the adjacent phases and the capacitance of the phase to substrate. For example, the total capacitance on phase A1 is 2 times 10 nF plus 20 nF for a total of 40 nF.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. Specifically, the voltage for the amplifier and dump drains (pins 20, 21, 22, 29, 35, 36 and 37) must never be taken negative with respect to the substrate. Hence, if the substrate is to be operated at a positive voltage (e.g. to minimise dark current) then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero.

It is also important to ensure that excess currents (see note 16) do not flow in the OS or DOS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

Similarly, for powering down, the substrate must be taken to zero voltage before the drains.

POWER CONSUMPTION

The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from the parallel and serial clocking (i.e. driving the capacitive loads).

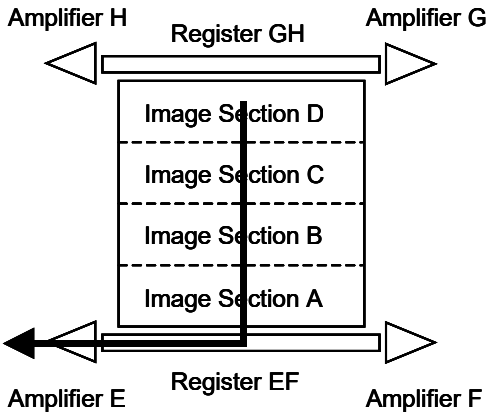
The table below gives representative values for the components of the on-chip power dissipation for the case of continuous split-frame line-by-line readout using both registers and all the output circuits with both real and dummy amplifiers activated. The frequency is that for clocking the serial register and an appropriate value of the amplifier load is utilised in each case.

Readout frequency	Line time	Amplifier load	Power dissipation			
			Amplifiers	Serial clocks	Parallel clocks	Total
100 kHz	21 ms	10 kΩ	165 mW	17 mW	3 mW	185 mW
1 MHz	2.2 ms	5 kΩ	275 mW	170 mW	30 mW	475 mW
3 MHz	800 µs	2.2 kΩ	525 mW	510 mW	90 mW	1,125 mW

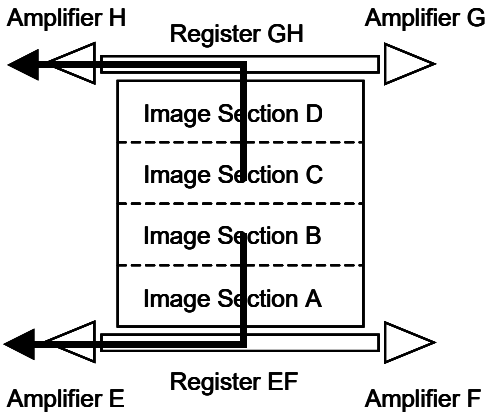
The dissipation reduces to only that of the amplifiers during the time that charge is being collected in the image sections with both parallel and serial clocks static.

FRAME READOUT MODES

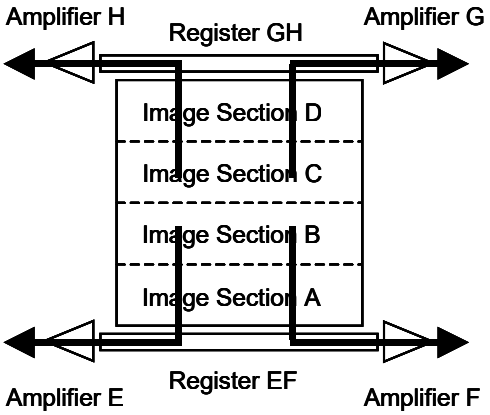
The device can be operated in a full-frame or split full-frame mode with readout from one, two or four amplifiers. These modes are determined by the clock pulse sequences applied to the image and register clocks. The diagrams below show some of the transfer options that are possible.



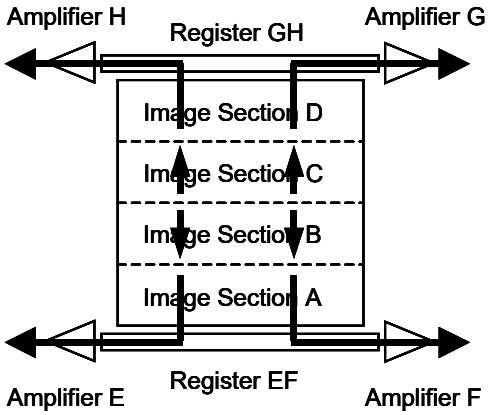
Full frame read-out through one amplifier



Split full frame read-out through two amplifiers



Split full frame read-out through four amplifiers



Split frame transfer through four amplifiers

If the applied drive pulses are designated IØ1, IØ2, IØ3 and IØ4, then connections should be made as tabulated below to affect the following directions of transfer.

	IØ1	IØ2	IØ3	IØ4	
A section transfer towards E-F register	A1	A2	A3	A4	TGA = IØ4
B section transfer towards E-F register	B1	B2	B3	B4	
C section transfer towards G-H register	C1	C2	C3	C4	
D section transfer towards G-H register	D1	D2	D3	D4	TGD = IØ1
A section transfer towards G-H register	A4	A3	A2	A1	TGA = “low”
B section transfer towards G-H register	B4	B3	B2	B1	
C section transfer towards E-F register	C4	C3	C2	C1	
D section transfer towards E-F register	D4	D3	D2	D1	TGD = “low”

The first four transfer sequences are for split frame readout. The second four are for reversing the transfer direction in either section for readout to only one of the registers. For example, using sequences 1, 2, 7 and 8 reads the whole device out through register E-F.

Transfer from the image section to the register is into the phase 1 and 2 electrodes, i.e. E1, F1, G1, H1, E2, F2, G2 and H2. These electrodes must be held at clock “high” level during the process. If the register pulses are designated RØ1, RØ2 and RØ3, then connections should be made as tabulated below to affect the following directions of transfer.

Clock Generator Drive Pulse Name	RØ1	RØ2	RØ3
E section transfer towards E output	E2	E1	E3
F section transfer towards F output	F2	F1	F3
G section transfer towards G output	G2	G1	G3
H section transfer towards H output	H2	H1	H3
E section transfer towards F output	E1	E2	E3
F section transfer towards E output	F1	F2	F3
G section transfer towards H output	G1	G2	G3
H section transfer towards G output	H1	H2	H3

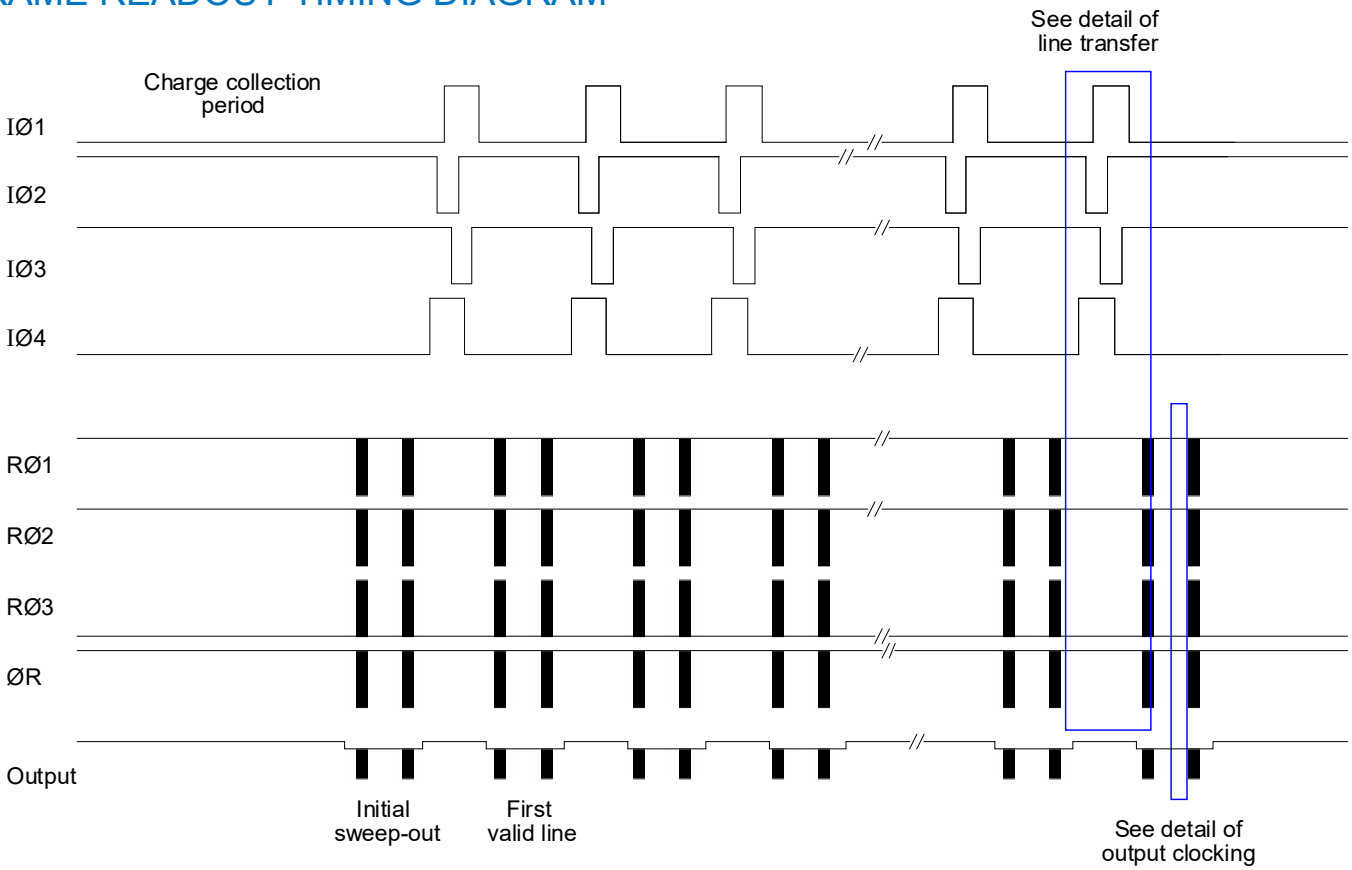
The first four sequences are for split register readout to all four outputs. The second four are for the reversal of direction in any half-section.

The last electrode before the output gate is separately connected to give the function of a summing well (SW). In normal readout (i.e. if not used for summing), SW is clocked as RØ3. For summing, the selected SW gate is held at clock “high” level for the required number of readout cycles, and then clocked as RØ3 to output charge.

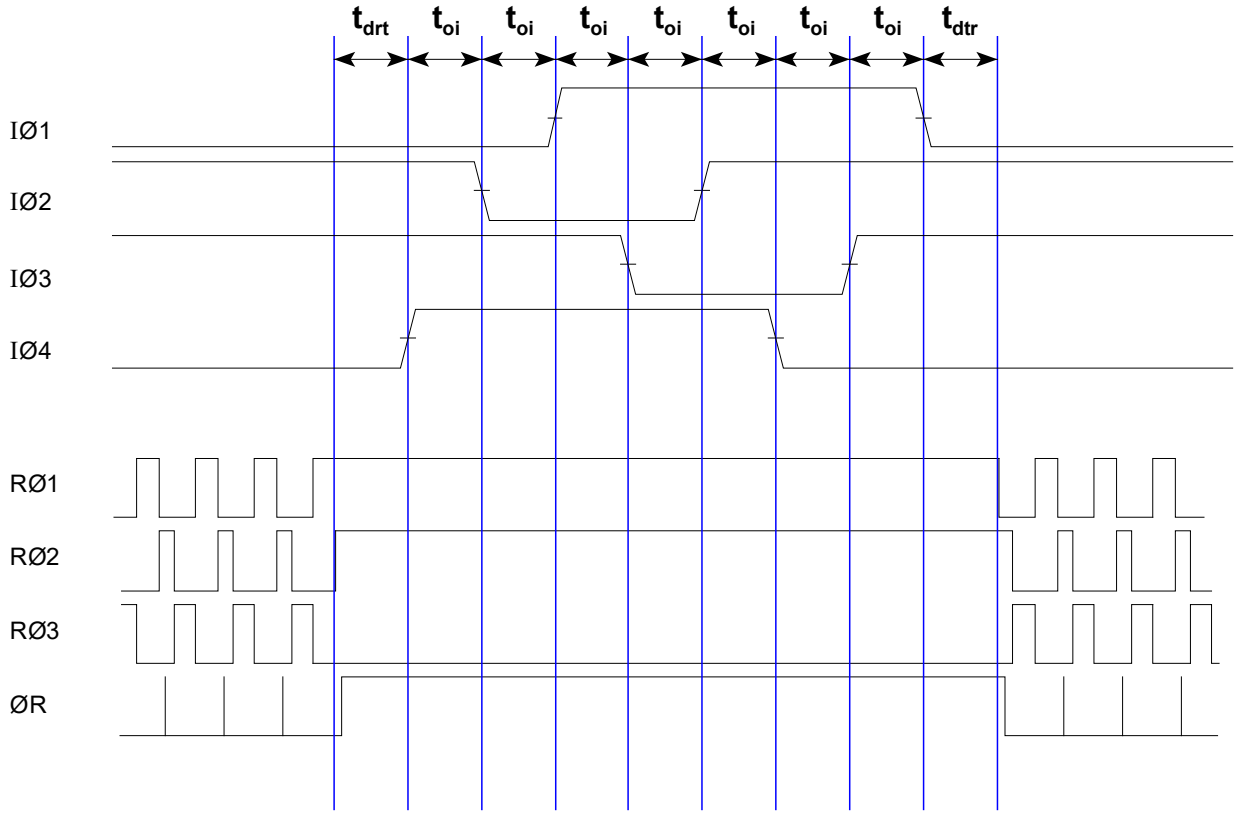
Alternatively, SW may be operated as a second output gate to provide the option of operation in low gain/high signal mode (mode 2) with OG high. If this mode of operation is used, then the sequencing of the output clocks must be changed, as charge now transfers into the output node as RØ2 goes low (see notes 3 and 17).

Image phases 2 and 3 should be held high during signal collection, as shown in the following figures.

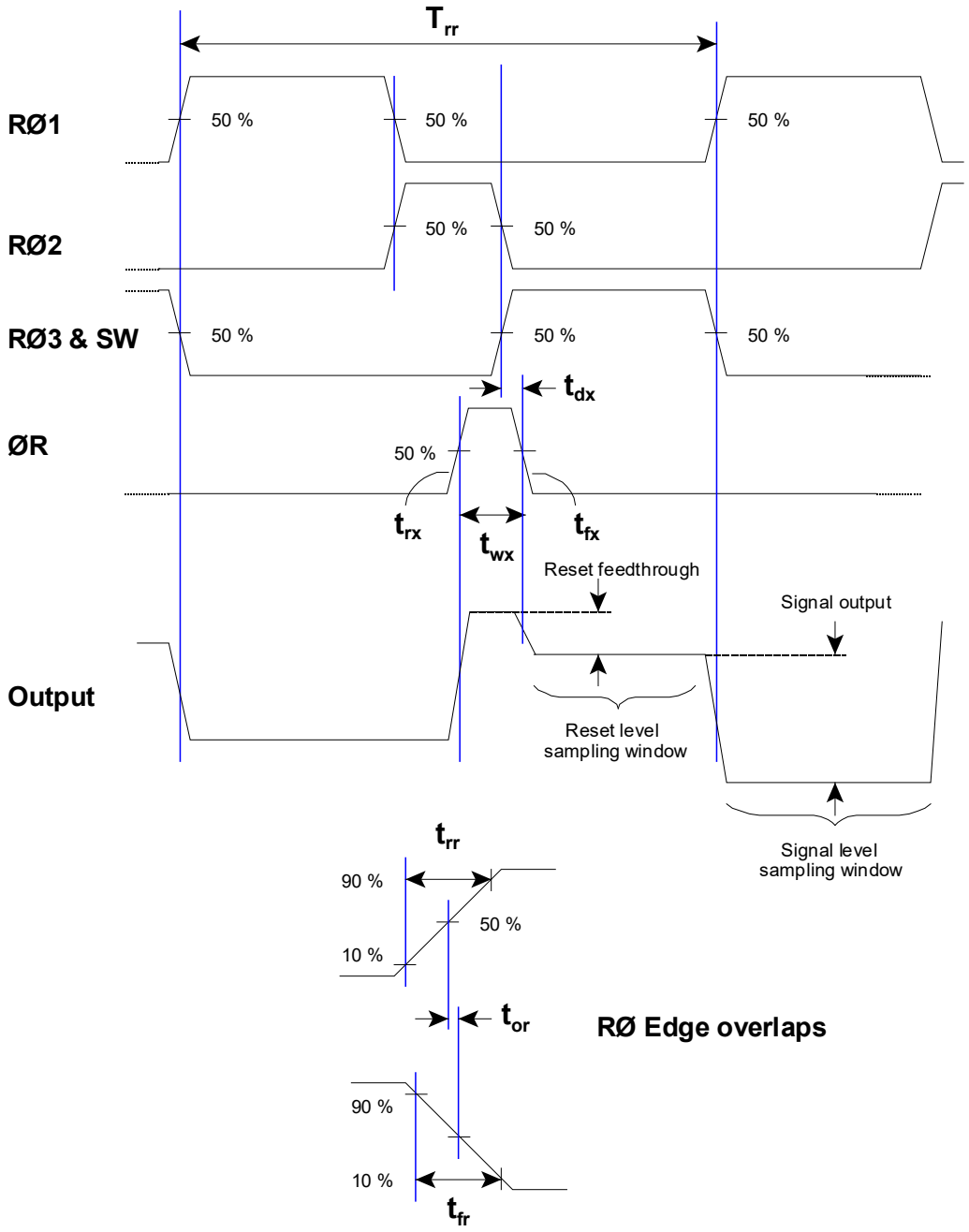
FRAME READOUT TIMING DIAGRAM



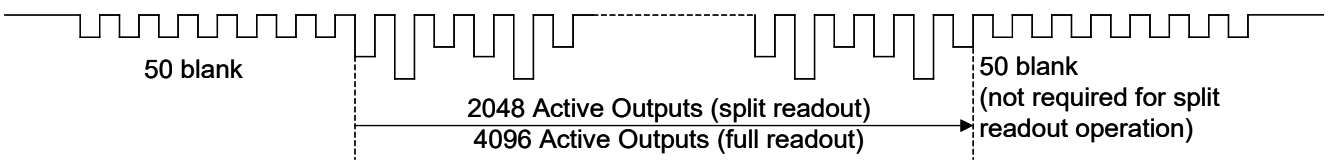
DETAIL OF LINE TRANSFER



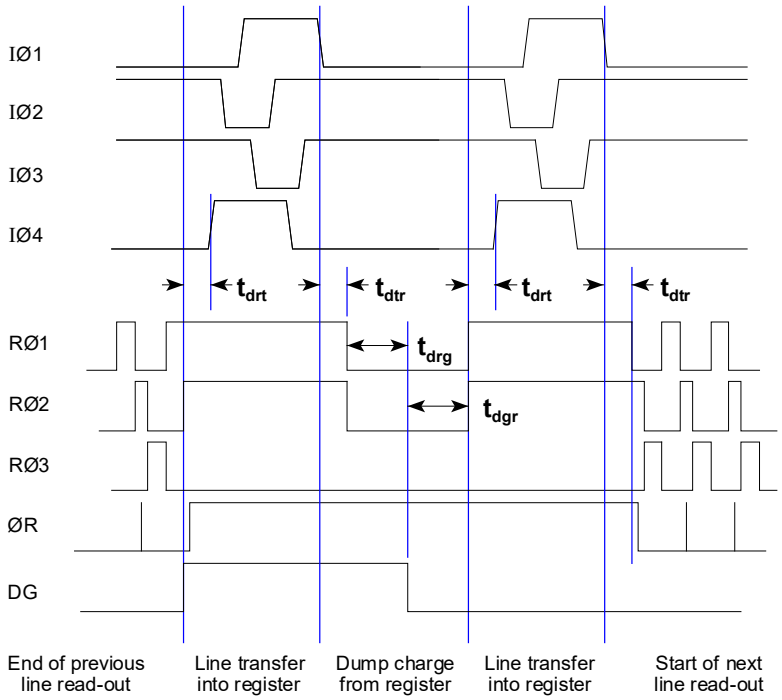
DETAIL OF OUTPUT CLOCKING (with SW clocked as RØ3)



LINE OUTPUT FORMAT



DETAIL OF VERTICAL LINE TRANSFER (Single line dump)



CLOCK TIMING REQUIREMENTS

Symbol	Description	Minimum	Typical	Maximum	Units
T_i	Line transfer time (see note 21)	65	75	(see note 23)	µs
t_{oi}	Image clock pulse edge overlap	7.5	10	(see note 23)	µs
t_{ri}	Image clock and transfer gate pulse rise time	1	1	0.3 t_{oi}	µs
t_{fi}	Image clock pulse fall time	1	1	0.3 t_{oi}	µs
t_{drt}	Delay time, RØ stop to IØ rising	5	10	(see note 23)	µs
t_{dtr}	Delay time, IØ falling to RØ start	7.5	10	(see note 23)	µs
t_{drg}	Delay time, RØ falling to DG rising	10	10	N/A	µs
t_{dgr}	Delay time, DG falling to RØ rising	7.5	10	N/A	µs
T_{rr}	Register clock period (see notes 24 and 25)	300	2000	(see note 23)	ns
t_{rr}	Register clock pulse rise time	10	50	0.05T_{rr}	ns
t_{fr}	Register clock pulse fall time	10	50	0.05T_{rr}	ns
t_{or}	Register clock pulse edge overlap	0	50	0.05T_{rr}	ns
t_{wx}	Reset pulse width (see note 22)	>3 t_{rx}	300	0.2T_{rr}	ns
t_{rx}	Reset pulse rise time	10	40	50	ns
t_{fx}	Reset pulse fall time	10	40	50	ns
t_{dx}	Delay time, RØ falling to ØR falling	10	100	0.05T_{rr}	ns

NOTES

21. Generally, $T_i = t_{drt} + 7t_{oi} + t_{dtr}$.

22. The RØ2 pulse-width is normally minimised, as shown, such that the RØ1 and RØ3 pulse widths can be increased to maximise the output reset and signal sampling intervals.

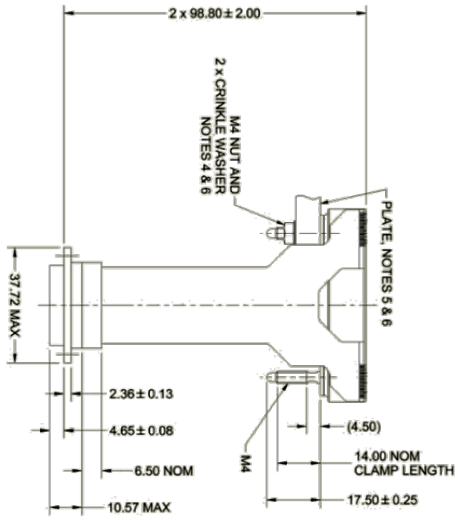
23. As set by any system specifications.

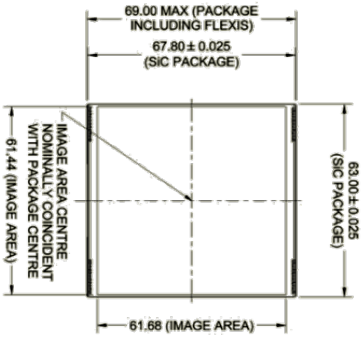
24. The typical timing is for readout at frequencies in the region of 500 kHz.

25. For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz, then the load may be increased to 10 kΩ to reduce power consumption. See also note 5. Operation at highest speed has not been factory tested.

OUTLINE DRAWINGS

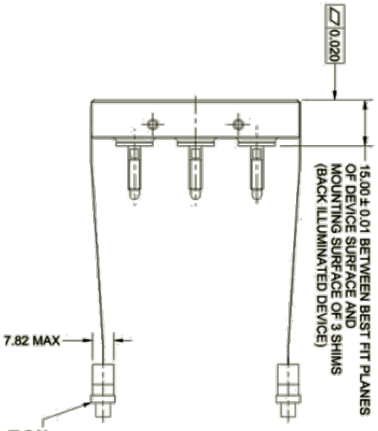
All dimensions shown in mm. Dimensions without limits are nominal. Package detail – A. Buttable Package

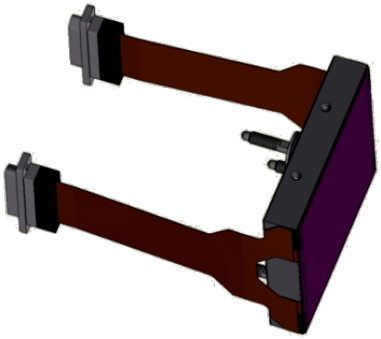


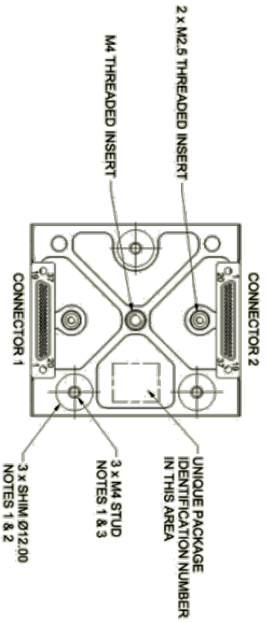


NOTES:

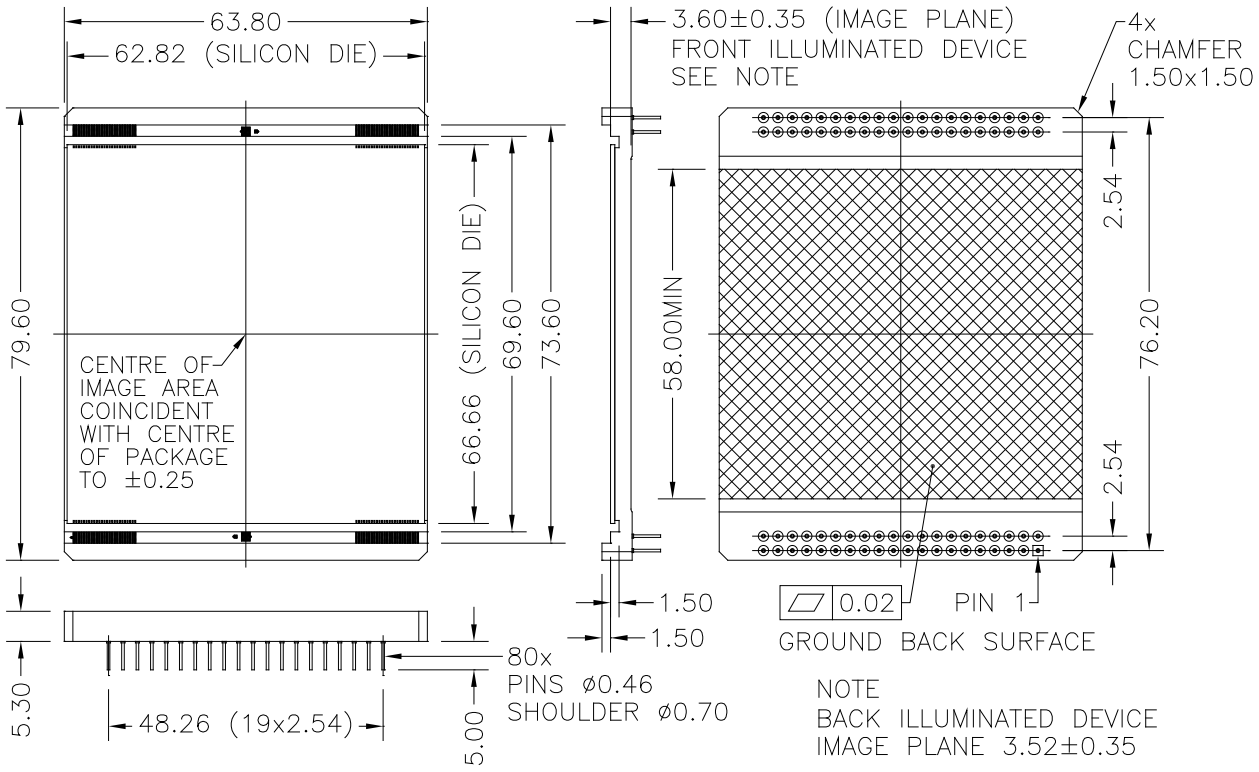
1. DO NOT REMOVE STUDS AND SHIMS.
2. SHIMS: INVAR 36 WITH FINE GROUND FINISH.
3. STUDS: INVAR 36.
4. RECOMMENDED COMPRESSION OF THE CRINKLE WASHERS IS ACHIEVED BY TIGHTENING THE 3 x M4 NUTS UNTIL FINGER TIGHT (6cN.m APPROX) AND THEN EACH BY A FURTHER 90° +10° -0°.
5. MOUNTING PLATE, THICKNESS: 8.00 TYP (5.00 MIN, 10.00 MAX).
6. ITEMS TO BE SUPPLIED BY CUSTOMER.







Package detail – B. Ceramic PGA Package



26. Two NTC BC302J6N thermistors are provided in the package for thermal control purposes.

HEALTH AND SAFETY HAZARDS

Teledyne e2v devices are safe to handle and operate, provided that the relevant precautions stated herein are observed. Teledyne e2v does not accept responsibility for damage or injury resulting from the use of devices it produces. Equipment manufacturers and users must ensure that adequate precautions are taken. Appropriate warning labels and notices must be provided on equipment incorporating Teledyne e2v devices and in operating manuals.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (i.e. all CCD pins except SS, DD, RD, OD and OS) but not to the other pins.

The devices are assembled in a clean room environment. Teledyne e2v recommend that similar precautions are taken to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising radiation. Users planning to use CCDs in a high radiation environment are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	148	-	373	K
Operating	153	-	323	K

Performance parameters are measured with the device at a temperature of 173 K and, as a result, full performance is only guaranteed at this nominal operating temperature.

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling..... 5 K/min

PART REFERENCES

Variant	Package	Illumination	Enhanced BSI Process	Silicon	AR Coating	Fringe Suppression
CCD231-84-G-141	SiC Buttable	BSI	Yes	Standard	Broadband	No
CCD231-84-G-D84	Ceramic-PGA	BSI	Yes	Standard	Broadband	No
CCD231-84-G-S77	SiC Buttable	BSI	Yes	Standard	Multi-19	No
CCD231-84-G-S76	Ceramic-PGA	BSI	Yes	Standard	Multi-19	No
CCD231-84-G-E56	SiC Buttable	BSI	Yes	Standard	Midband	No
CCD231-84-G-E58	Ceramic-PGA	BSI	Yes	Standard	Midband	No
CCD231-84-G-G57	SiC Buttable	BSI	Yes	Standard	Multi-2	No
CCD231-84-G-G85	Ceramic-PGA	BSI	Yes	Standard	Multi-2	No
CCD231-84-G-H34	SiC Buttable	BSI	Yes	Standard	No Coat	No
CCD231-84-G-H33	Ceramic-PGA	BSI	Yes	Standard	No Coat	No
CCD231-84-G-E74	SiC Buttable	BSI	Yes	Deep Depletion	Multi-2	Yes
CCD231-84-G-F21	Ceramic-PGA	BSI	Yes	Deep Depletion	Multi-2	Yes
CCD231-84-G-H69	SiC Buttable	BSI	Yes	Deep Depletion	Multi-15	Yes

Grade Definitions

Grade 0	Super Grade	Meets all Grade 0 performance parameters and cosmetic parameters
Grade 1	Science Grade	Meets all Grade 1 performance parameters and cosmetic parameters
Grade 2	Low Science Grade	Meets all Grade 2 performance parameters and cosmetic parameters. Grade 2 have limited availability and offered on a case-by-case basis.
Grade 5	Engineering Grade	Electrically functional with no performance or cosmetic parameter guarantees
Grade 6	Mechanical Grade	Non-functional. Mechanically representative only.

NOTES

27. G = Grade (e.g. 1)
28. Additional variants may be available to custom order. Consult Teledyne e2v for more information.