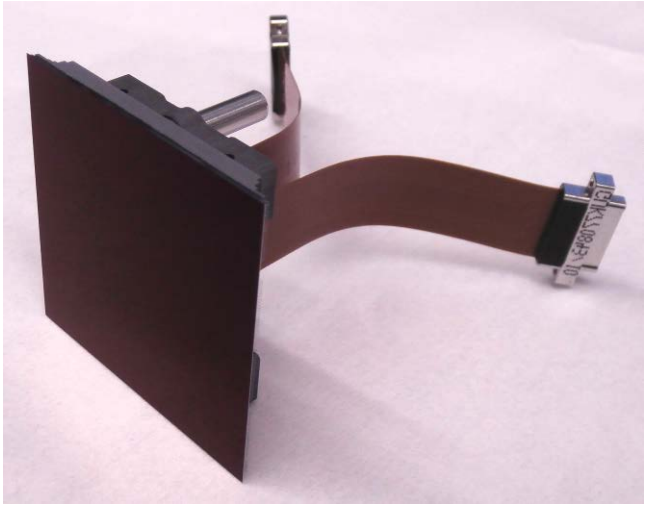
CCD250-82 NIMO Back Illuminated High-Rho High Performance CCD Sensor

FEATURES

- Enhanced Infrared Sensitivity – using thick high resistivity silicon
- 4096 by 4004 Pixel Format
- 10µm Square Pixels
- Active image area 41 mm x 40 mm
- 4-side buttable format for mosaic construction
- Back Illuminated for high quantum efficiency
- Non-Inverted Mode Operation (NIMO)



INTRODUCTION

The CCD250-82 is a split frame sensor with an image area of 4096 x 4004 pixels and 16 outputs for faster readout. Back illumination technology, in combination with an extremely low noise amplifier, makes the device well suited to the most demanding applications, such as astronomy.

The 'High-Rho' technology is used to increase the thickness of the silicon to extend the response significantly at the infra-red end of the spectral range. The device operates in the same manner as other Teledyne e2v sensors, but with additional back-substrate bias voltage to fully deplete the silicon. Details are given at the end of this datasheet.

The device is supplied in a package designed to facilitate the assembly of large close-butted mosaics used at cryogenic temperatures. The design of the package ensures that it is 4 sides buttable and that the device flatness is maintained at the working temperature.

Designers are advised to consult Teledyne e2v should they be considering using CCD sensors in abnormal environments or if they require customised packaging or performance features.

TYPICAL PERFORMANCE

Pixel readout frequency	550 kHz
Output amplifier sensitivity	6.5 µV/e^-
Peak signal	135 ke^-/pixel
Spectral range	300–1100 nm
Readout noise @ 550 kHz	5.0 e^- rms

GENERAL DATA

Format

Silicon die size	42 x 42 mm
Active pixels	4096 (H) x 4004 (V)
Pixel size	10µm square
Number of output amplifiers	16

Package

Package footprint	42 x 42 mm
Flatness	≤7 µm Peak to Valley
Focal plane height	13.00mm ± 10µm
Package type	Buttable ceramic with two 37 way nanominiature flexi connector plugs

Whilst Teledyne e2v has taken care to ensure the accuracy of the information contained herein it accepts no responsibility for the consequences of any use thereof and also reserves the right to change the specification of goods without notice. Teledyne e2v accepts no liability beyond that set out in its standard conditions of sale in respect of infringement of third party patents arising from the use of tubes or other devices in accordance with information contained herein.

Teledyne e2v (UK) Limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom Teledyne e2v (UK) Ltd. is a Teledyne Technologies company.
Telephone: +44 (0)1245 493493 Facsimile: +44 (0)1245 492492
Contact Teledyne e2v by e-mail: Enquiries@Teledyne-e2v.com or visit www.teledyne-e2v.com for global sales and operations centres.

© Teledyne e2v (UK) Limited 2018

ELECTRO-OPTICAL PERFORMANCE (At 178K unless stated)

		Min	Typical	Max	Units	Note
Image peak charge storage		120,000	135,000	-	e^-/pixel	
Register peak charge storage		-	195,000	-	e^-/pixel	1
Output amplifier responsivity		-	6.5	-	µV/e^-	2
Readout noise		-	5	8	rms e^-	3
Readout frequency		-	550	-	kHz	4
Dark signal		-	0.02	0.1	e^-/pixel/s	5
Charge transfer efficiency	Parallel	99.999	99.9995	-	%	6
	Serial	99.999	99.9995	-	%	
Image area flatness (peak to valley)		-	3	7	µm	7

NOTES

1) Predicted values from design; not measured.
2) Responsivity increases by approximately 5% as BSS changes from 0V to -70V.
3) Measured with digital correlated double sampling at 550 kHz pixel rate, in darkness and reverse clocking the register clocks to exclude dark signal shot noise.
4) All factory testing is performed at the typical 550 kHz readout frequency. The maximum frequency of the output depends on the external load capacitance to be driven but is expected to be > 1 MHz, though this is not verified by test. The register will transfer charge at higher frequencies, but performance cannot be guaranteed.
5) Dark signal is typically measured at 178K. It is a strong function of temperature and the typical average (background) dark signal is taken as:
$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$
where Q_{d0} is the dark current at 293 K. In some circumstances strong illumination may leave a low level of residual charge in the following image; this may be minimised by inverting parallel clocks prior to exposure; raise VFSS to +9 with all image clocks (temporarily) at low levels (0V) for a minimum duration of 150ms.
6) The CTE value is quoted for the complete clock cycle (i.e. not per phase).
7) Mechanical parameters are measured at room temperature, however flatness is guaranteed at 173K with compliance predicted from models.

Effects of increased thicknesses

The CCD250-82 default thickness is 100 µm. This increased device thickness, compared to standard Teledyne e2v sensors, provides increased long-wavelength sensitivity as shown above. This comes at the penalty of increased detection of cosmic rays, which can limit long exposures. In order to attain best point spread function (or MTF), a back bias voltage (BSS) is required, as discussed later. If this value is too high then some increase in white defects may be seen, and so there can be a trade-off between this effect and that of optimum PSF.

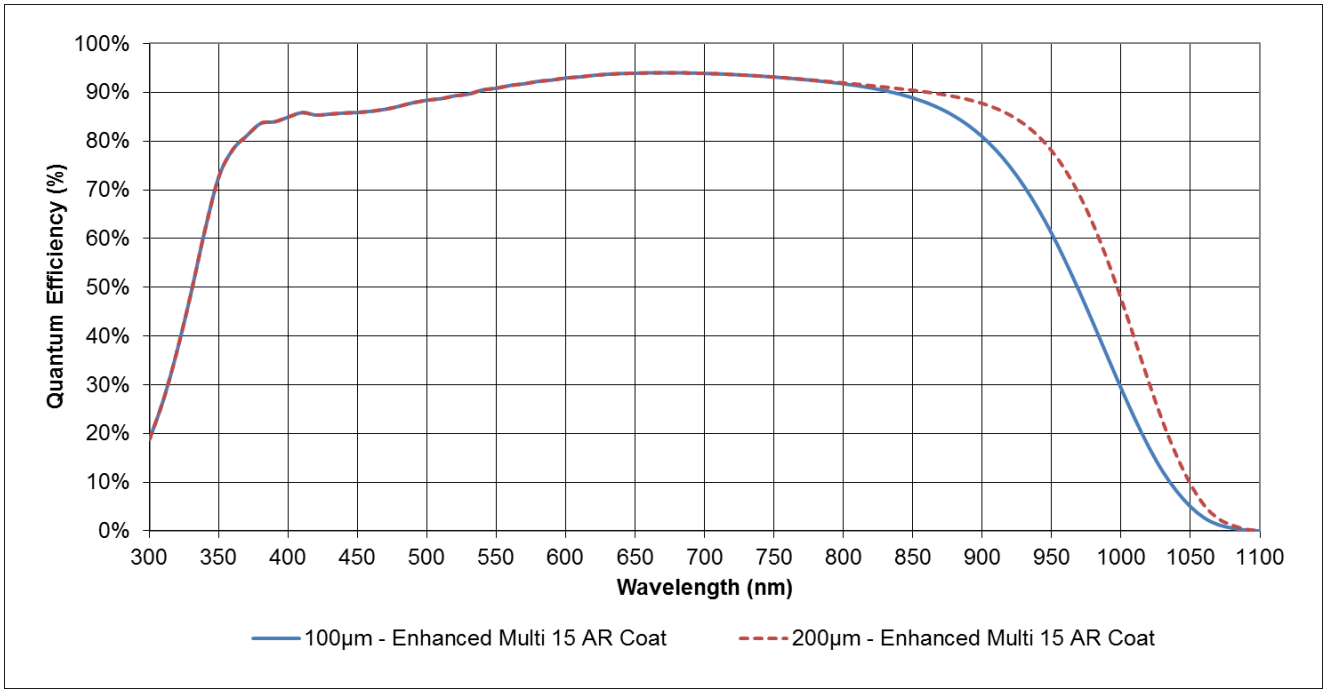
Devices with increased thickness could be supplied to custom order; contact factory for information.

All performance parameters (as above) are measured with VBSS set to -70V.

SPECTRAL RESPONSE AT 178K

Wavelength (nm)	Minimum QE (%)	Maximum Response Non-uniformity (1σ)(%)
	Enhanced Process Multi-15 AR Coating	
350	55	5
450	80	3
500	80	3
620	85	3
750	85	3
870	80	3
1000	20	5

TYPICAL SPECTRAL RESPONSE CURVE AT 178K



The 200µm thick silicon version is available to custom order upon request

COSMETIC SPECIFICATION

Maximum allowed defect levels are indicated below. Measured at a BSS of -70V.

GRADE	0	1	2
Column defects; Black or White	2	20	40
White spots	20	200	800
Black spots	50	400	800
Traps >200 e^-	20	40	80

There is some dependence on BSS; indications are that defect count increases for highest values of BSS. This is associated with device thickness; as described above. Specification levels apply at the typical BSS value of -70V. This level is sufficient to fully deplete the device for full resolution (at nominal device thickness). A higher value of BSS can increase resolution slightly but at the expense of risk of more severe white pixel defects.

Grade 5 devices are also available as electrical samples. These are confirmed to have working outputs and will nominally provide an image. Not all parameters are guaranteed to be tested or provided and the image quality may be worse than that of a grade 2.

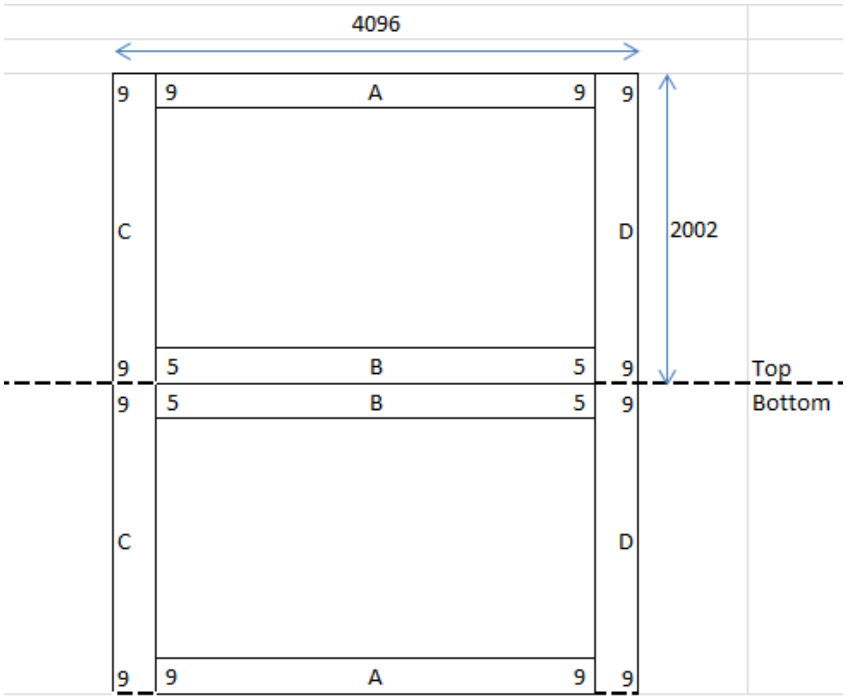
Grade 6 devices are also available as mechanical samples. No electrical performance is provided and these should not be connected to electronics. The mechanical performance parameters will be measured but not guaranteed to be compliant to the maximum values above.

DEFINITIONS

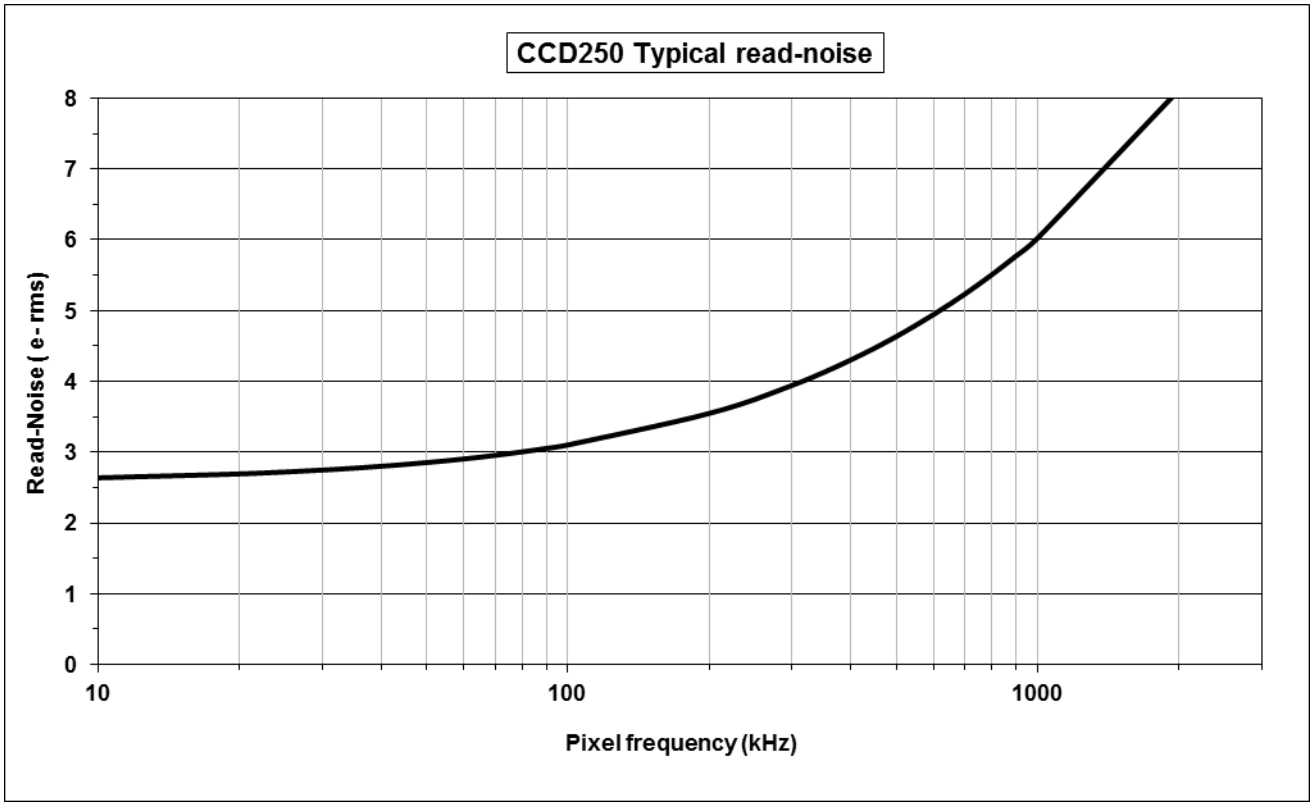
White spots	A pixel is counted as a white spot defect if the dark signal generation rate is more than 5 e-/s at 178K
Black spots	A black spot defect is a pixel with a 500nm photoresponse less than 80% of the local mean signal.
White Column defects	A column is counted as a defect if it contains at least 20 contiguous white single pixel defects.
Black Column defects	A column is counted as a defect if it contains at least 100 contiguous black single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e- at 178K

EXCLUSION ZONES

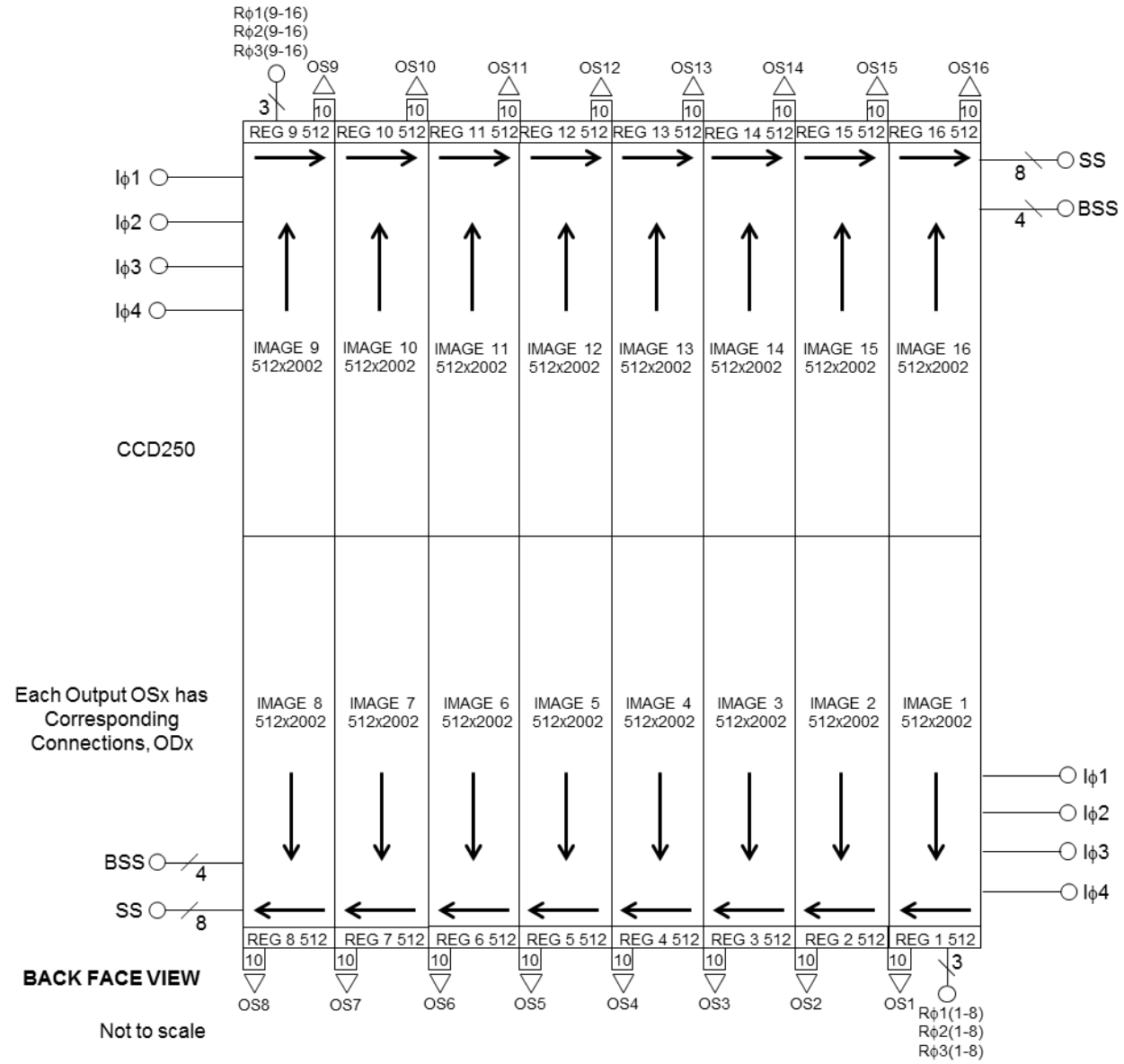
The first 9 rows and last 5 rows are excluded from defect assessment. Also, due to the edge effects associated with the hi-rho technology, the first 9 and last 9 columns are also excluded from photo response defect and PRNU assessment, as indicated below. This edge effect exhibits as some “roll off“ of sensitivity of the edges of the device.



TYPICAL OUTPUT CIRCUIT NOISE

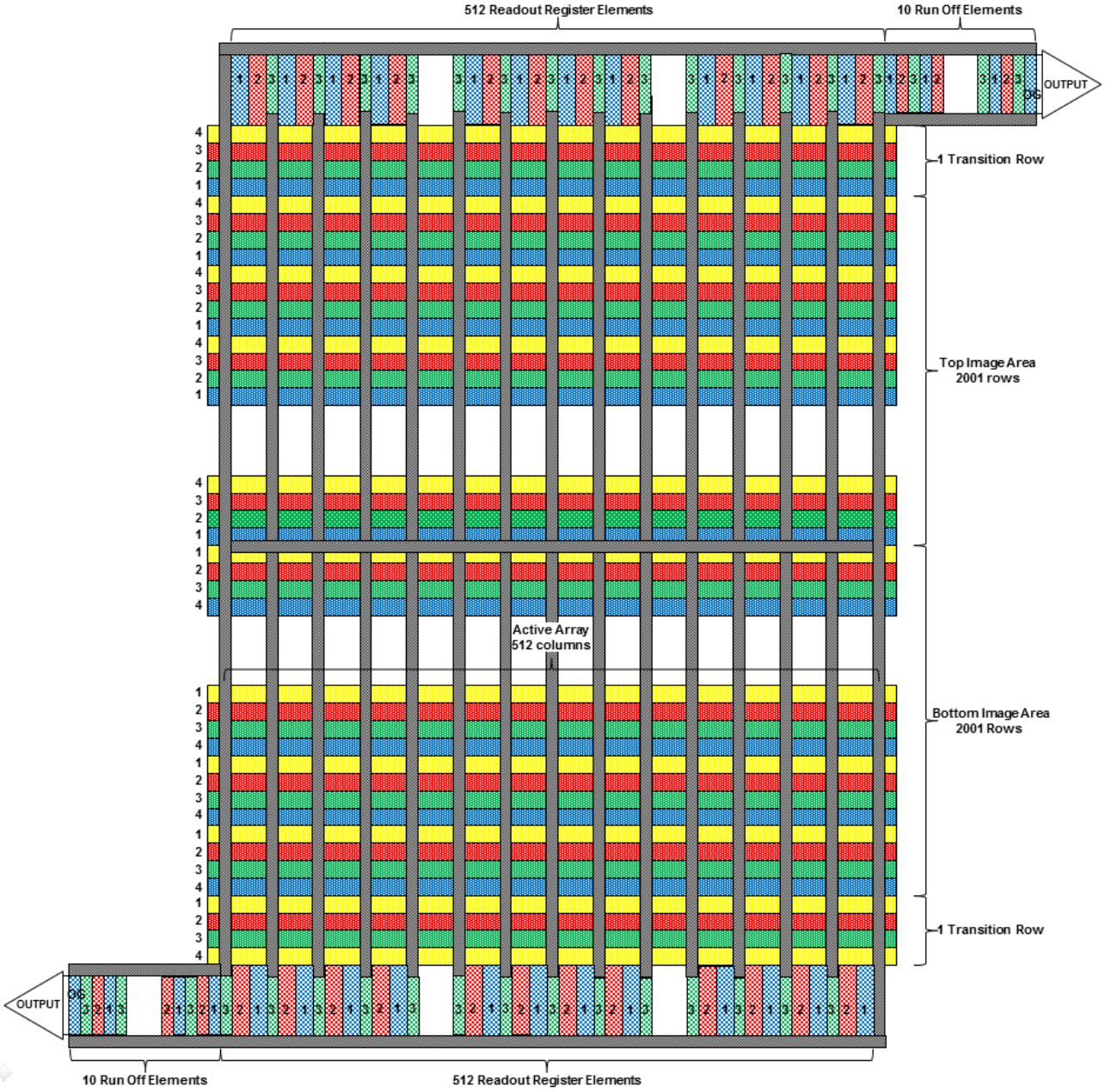


DEVICE SCHEMATIC



Not all connections are shown.

DEVICE ELECTRODE SCHEMATIC



ELECTRICAL INTERFACE

FLEX CONNECTOR 1

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 9)			MAX RATINGS with respect to FSS
			Min	Typical	Max	
1	BSS	Back Substrate (see note 8)	-70	-70	0	-70V
2	OD1	Output Drain 1	0.2	30	32	–0.3 to +35V
3	OD2	Output Drain 2	0.2	30	32	–0.3 to +35V
4	OD3	Output Drain 3	0.2	30	32	–0.3 to +35V
5	OD4	Output Drain 4	0.2	30	32	–0.3 to +35V
6	RD	Reset Drain	0.2	18	20	–0.3 to +35V
7	TS	Temperature Sensor (see note 11)				-
8	IØ4	Image Section, phase 4 (clock pulse)	0	9	11	±20V
9	IØ2	Image Section, phase 2 (clock pulse)	0	9	11	±20V
10	TS	Temperature Sensor (see note 11)				-
11	RØ1	Reset register, phase 1 (clock pulse)	0.5	9.5	10	±20V
12	RØ3	Reset register, phase 3 (clock pulse)	0.5	9.5	10	±20V
13	TS	Temperature Sensor (see note 11)				-
14	OG	Output Gate	0	4	5	±20V
15	OD5	Output Drain 5	0.2	30	32	–0.3 to +35V
16	OD6	Output Drain 6	0.2	30	32	–0.3 to +35V
17	OD7	Output Drain 7	0.2	30	32	–0.3 to +35V
18	OD8	Output Drain 8	0.2	30	32	–0.3 to +35V
19	BSS	Back Substrate (see note 8)	-70	-70	0	-70V
20	FSS	Front Substrate	0	0	0.5	N/A
21	OS1	Output transistor source 1				N/A
22	OS2	Output transistor source 2				N/A
23	OS3	Output transistor source 3				N/A
24	OS4	Output transistor source 4				N/A
25	FSS	Front Substrate	0	0	0.5	N/A
26	GD	Guard Drain	0.2	26	30.5	–0.3 to +35V
27	IØ3	Image Section, phase 3 (clock pulse)	0	9	11	±20V
28	IØ1	Image Section, phase 1 (clock pulse)	0	9	11	±20V
29	ØR	Reset Gate	0	12	12	±20V
30	RØ2	Reset register, phase 2 (clock pulse)	0.5	9.5	10	±20V
31	GD	Guard Drain	0.2	26	30.5	–0.3 to +35V
32	FSS	Front Substrate	0	0	0.5	N/A
33	OS5	Output transistor source 5				N/A
34	OS6	Output transistor source 6				N/A
35	OS7	Output transistor source 7				N/A
36	OS8	Output transistor source 8				N/A
37	FSS	Front Substrate	0	0	0.5	N/A

FLEX CONNECTOR 2

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 9)			MAX RATINGS with respect to FSS
			Min	Typical	Max	
1	BSS	Back Substrate (see note 8)	-70	-70	0	-70V
2	OD9	Output Drain 9	0.2	30	32	–0.3 to +35V
3	OD10	Output Drain 10	0.2	30	32	–0.3 to +35V
4	OD11	Output Drain 11	0.2	30	32	–0.3 to +35V
5	OD12	Output Drain 12	0.2	30	32	–0.3 to +35V
6	OG	Output Gate	0	4	5	±20V
7	TS	Temperature Sensor (see note 11)				-
8	RØ3	Reset register, phase 3 (clock pulse)	0.5	9.5	10	±20V
9	RØ1	Reset register, phase 1 (clock pulse)	0.5	9.5	10	±20V
10	TS	Temperature Sensor (see note 11)				-
11	IØ2	Image Section, phase 2 (clock pulse)	0	9	11	±20V
12	IØ4	Image Section, phase 4 (clock pulse)	0	9	11	±20V
13	TS	Temperature Sensor (see note 11)				-
14	RD	Reset Drain	0.2	18	20	–0.3 to +35V
15	OD13	Output Drain 13	0.2	30	32	–0.3 to +35V
16	OD14	Output Drain 14	0.2	30	32	–0.3 to +35V
17	OD15	Output Drain 15	0.2	30	32	–0.3 to +35V
18	OD16	Output Drain 16	0.2	30	32	–0.3 to +35V
19	BSS	Back Substrate (see note 8)	-70	-70	0	-70V
20	FSS	Front Substrate	0	0	0.5	N/A
21	OS9	Output transistor source 9				N/A
22	OS10	Output transistor source 10				N/A
23	OS11	Output transistor source 11				N/A
24	OS12	Output transistor source 12				N/A
25	FSS	Front Substrate	0	0	0.5	N/A
26	GD	Guard Drain	0.2	26	30.5	–0.3 to +35V
27	RØ2	Reset register, phase 2 (clock pulse)	0.5	9.5	10	±20V
28	ØR	Reset Gate	0	12	12	±20V
29	IØ1	Image Section, phase 1 (clock pulse)	0	9	11	±20V
30	IØ3	Image Section, phase 3 (clock pulse)	0	9	11	±20V
31	GD	Guard Drain	0.2	26	30.5	–0.3 to +35V
32	FSS	Front Substrate	0	0	0.5	N/A
33	OS13	Output transistor source 13				N/A
34	OS14	Output transistor source 14				N/A
35	OS15	Output transistor source 15				N/A
36	OS16	Output transistor source 16				N/A
37	FSS	Front Substrate	0	0	0.5	N/A

NOTES

8) When the BSS is applied at -70V, it is necessary to have a minimum of 26V on the Guard Diode to guarantee back-front substrate isolation and prevent excessive current from flowing through the bulk silicon. See power up sequence on page 10.

9) If all voltages are set to the 'typical' values, operation at or close to specification should be obtained. Some adjustment within the minimum – maximum range specified may be required to optimise performance.

10) Voltage between pairs of pins: OS to OD + 15 V. Maximum current through any source or drain pin: 10 mA.

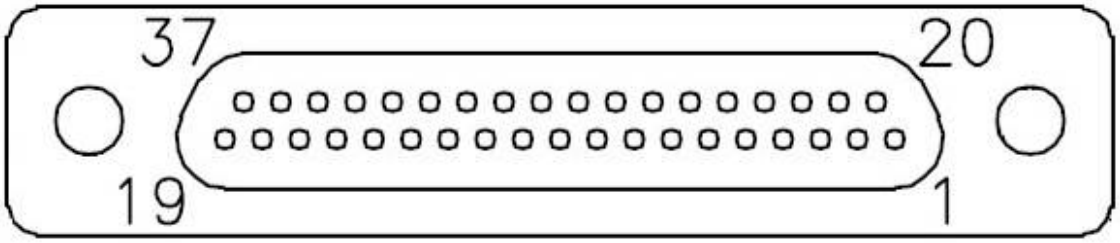
11) Temperature Sensor is a PT100.

TEMPERATURE SENSOR OPERATION

For 4 wire sense reading of the on chip PRT (PT100), see the connections below to get the most accurate readings of the sensor. The two pins marked N/C (Not connected) must be left floating and not connected to ground.

Connector	Pin	Function
1	7	Sense -
1	10	N/C
1	13	Sense +
2	7	N/C
2	10	Force +
2	13	Force -

PIN CONNECTIONS (View facing pins of connector)



This numbering applies to both connectors. The connectors are Glenair 37 Way, series 89 nanominiature plugs.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. This includes ensuring that reverse bias voltages cannot be momentarily applied.

The CCD has 2 substrates. The front substrate FSS for the output circuit is set to 0 V. The back substrate BSS is applied to the back surface of the CCD. To get full depletion a large negative potential is applied. A guard drain is designed to isolate front and back substrates.

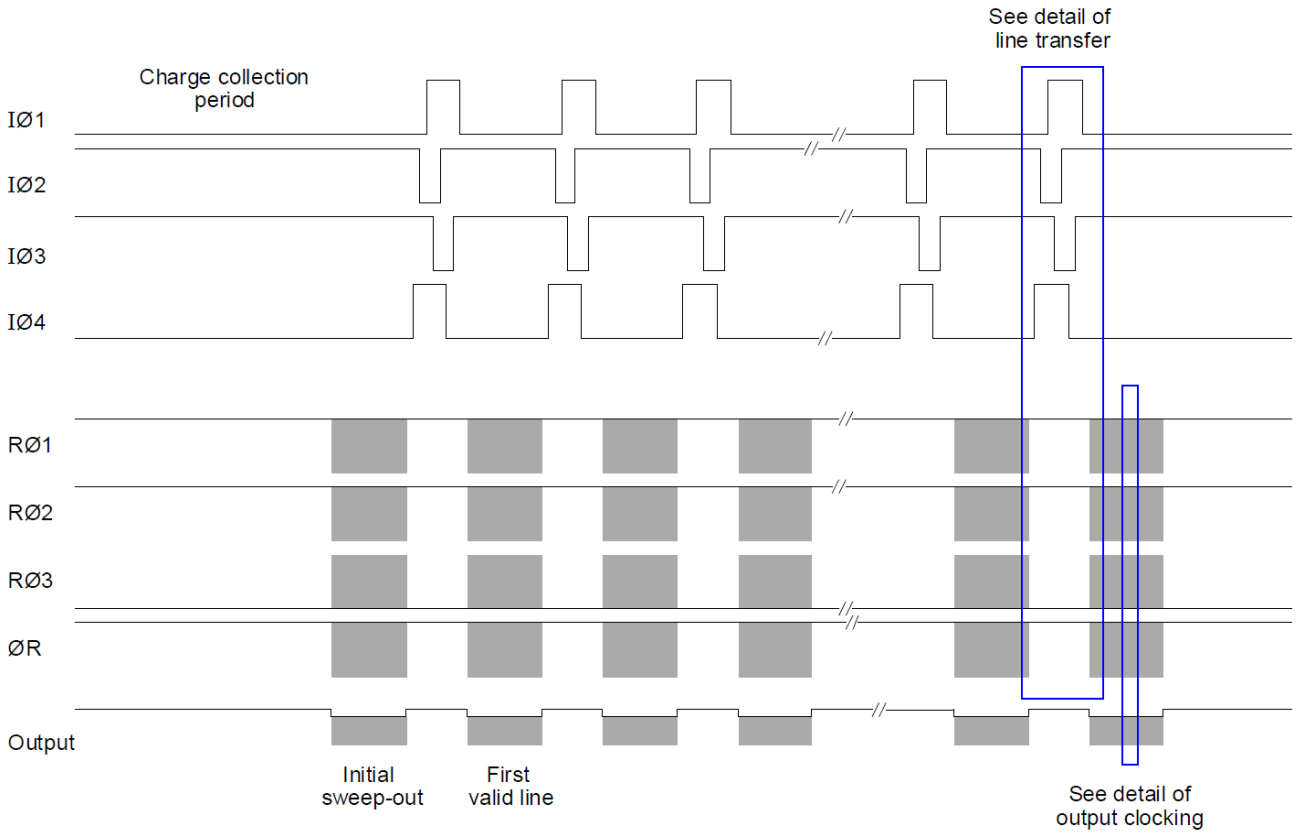
If there is a current flowing between FSS and BSS when switching on the guard drain, the insulation below the guard ring might not form properly. It is therefore advised to first set both FSS and BSS to 0V, then switch on the guard drain and all other biases and clocks in the order stated below, before applying any negative bias to BSS. The recommended power up order of all biases and clocks is listed in the table below.

BIAS/CLOCK	LABEL	POWER UP ORDER	Comment
Front Substrate	FSS	1	**Reference voltage 0 V**
Back Substrate	BSS	1	**Set to 0V at this stage**
Guard Drain	GD	2	
Reset Drain	RD	2	
Output Drain	OD	2	
Output Gate	OG	3	
Image Clock High	IØH	4	
Image Clock Low	IØL	4	
Register Clock High	RØH	4	
Register Clock Low	RØL	4	
Reset Gate High	ØRH	4	
Reset Gate Low	ØRL	4	
Back Substrate	BSS	5	**Set to desired voltage**

All levels must be settled before powering up the next group of biases. There can be a delay between the bias/clocks in any stated group.

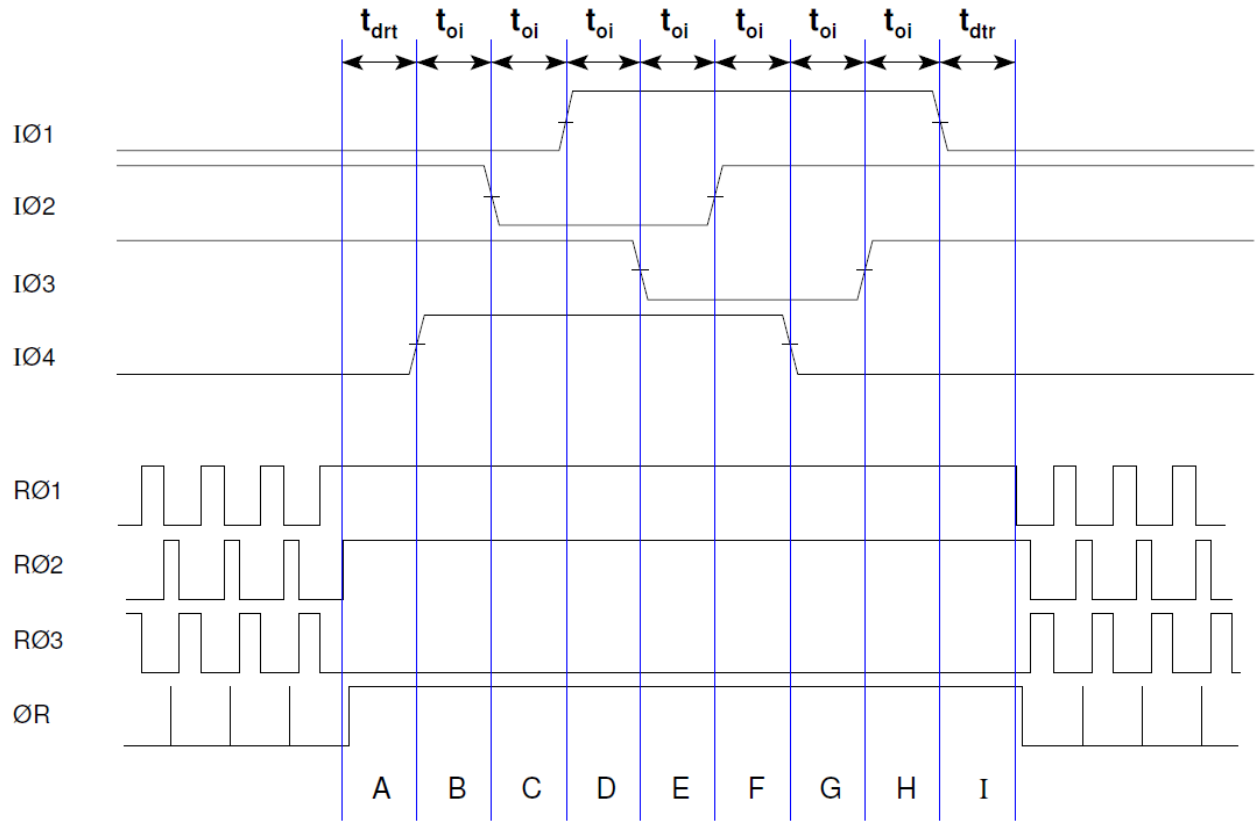
It is also important to ensure that excess currents do not flow in the OS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

FRAME READOUT TIMING DIAGRAM

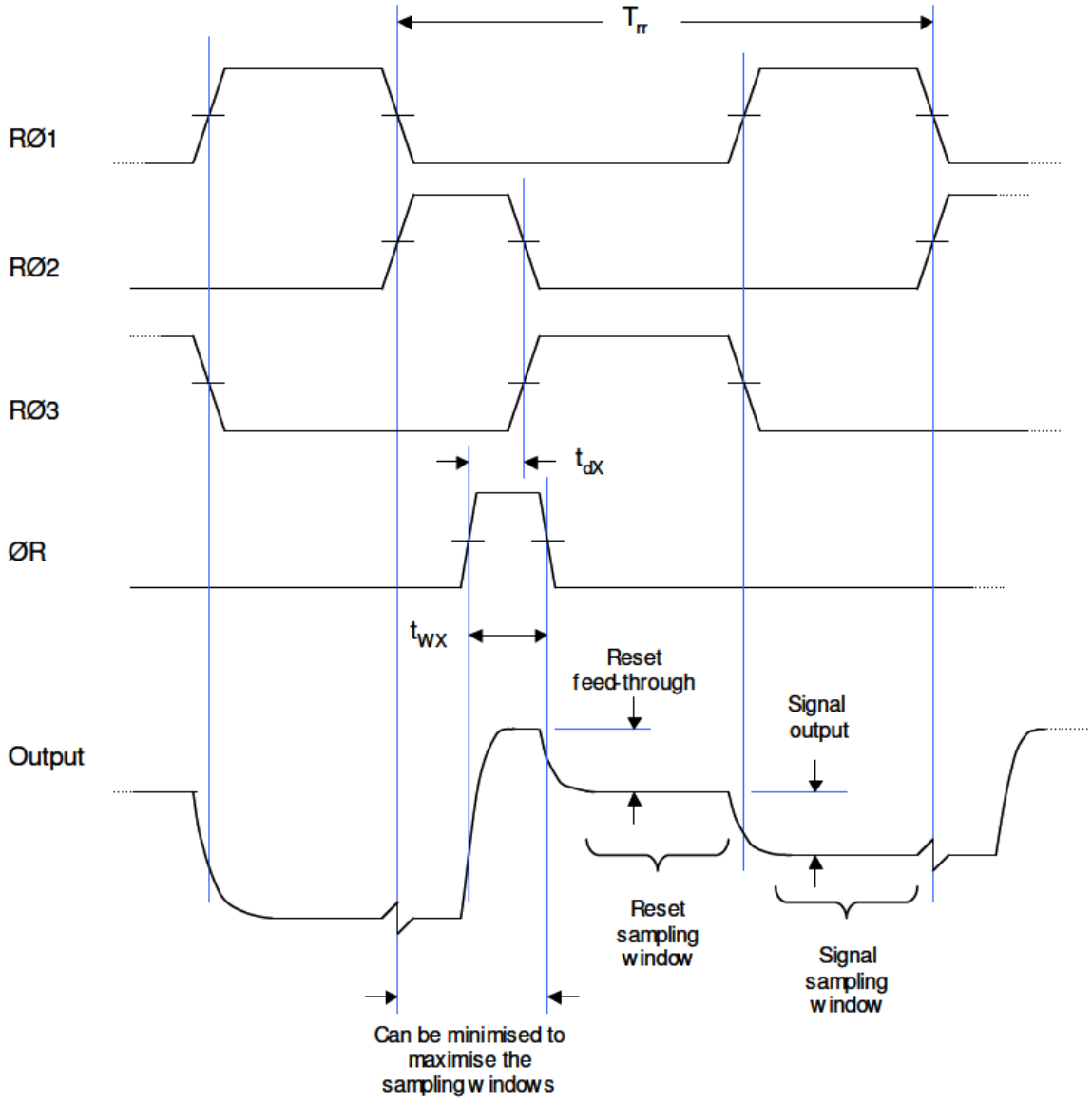


DETAIL OF LINE TRANSFER (Not to scale)

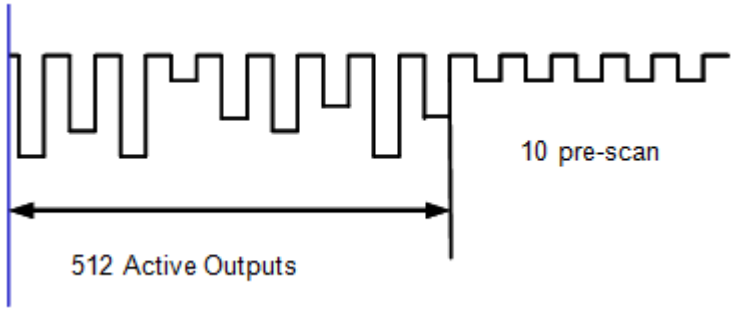
(For output from a single amplifier)



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



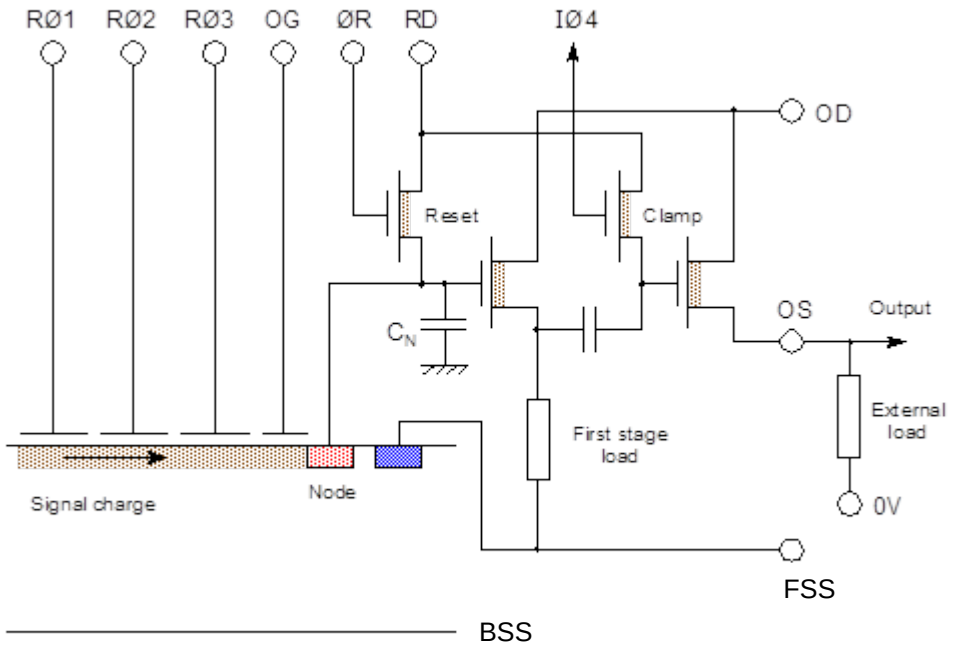
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typ	Max	Unit
T_i	Image clock period	10	12	See note 12	µs
t_{wi}	Image clock pulse width	5	8	See note 12	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.5	1	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	1	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	1	4	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	1	5	$0.2T_i$	µs
t_{dir}	Delay time, IØ stop to RØ start	3	9	See note 12	µs
t_{dri}	Delay time, RØ stop to IØ start	1	3	See note 12	µs
T_r	Output register clock cycle period	200	See note 13	See note 12	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.2T_r$	ns
t_{rx} , t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

12) No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
13) As set by the readout period. See note 4.

OUTPUT CIRCUIT

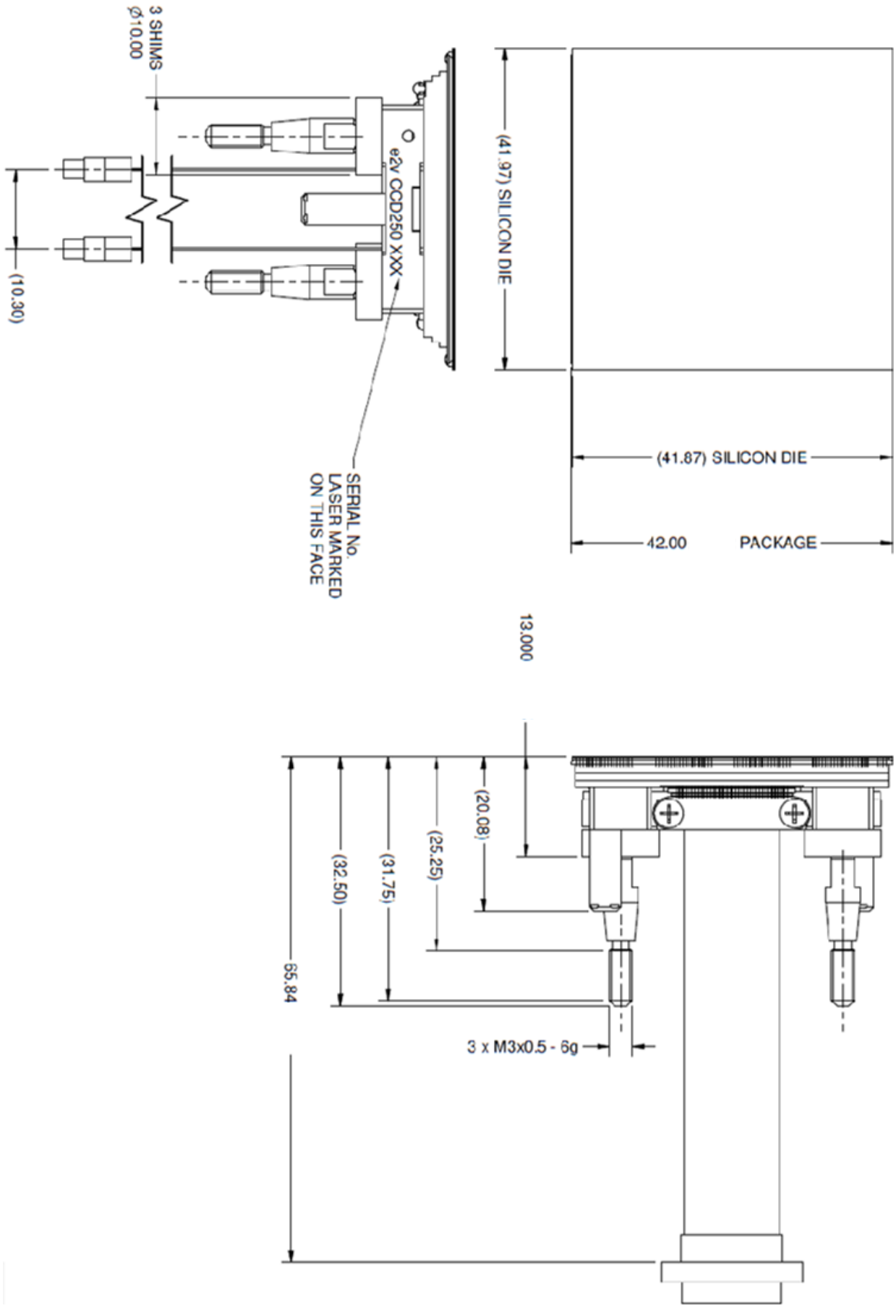


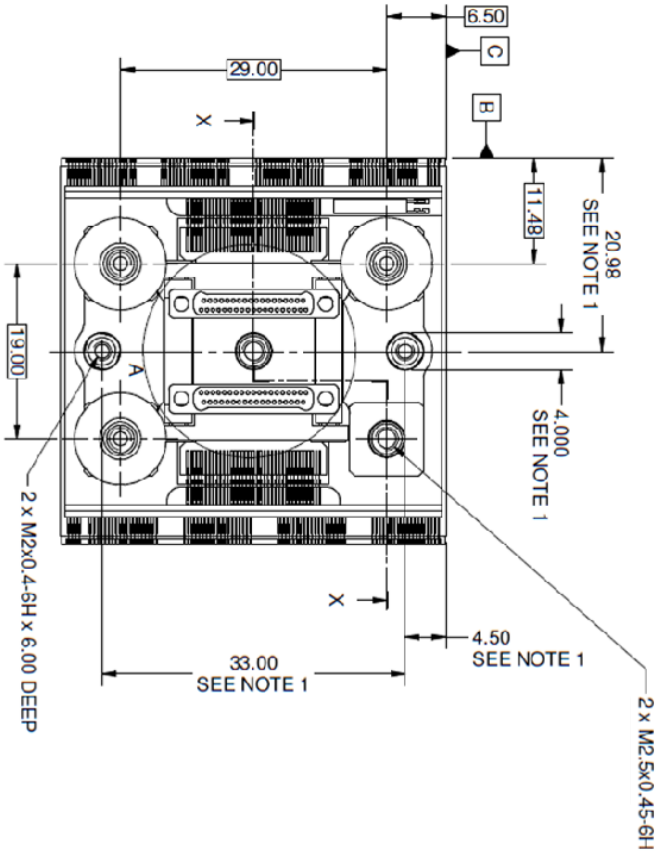
NOTES

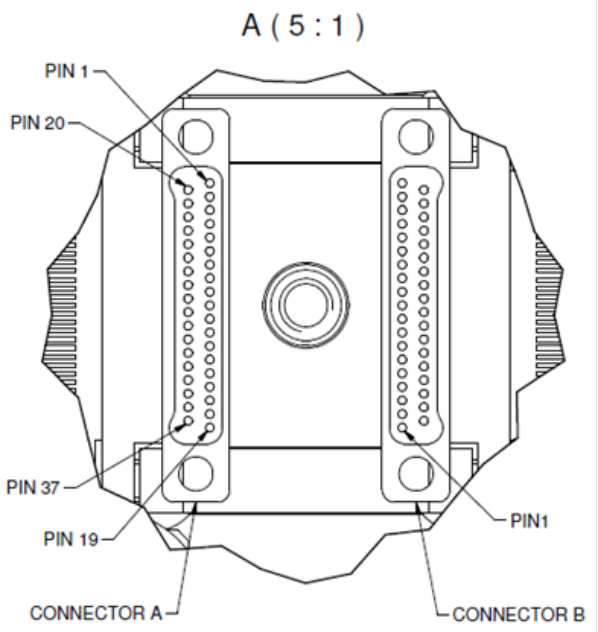
14) The amplifier has a DC restoration circuit, which is activated internally whenever IØ4 is pulsed high.
15) Output node capacity is typically 2 times that of the image section.

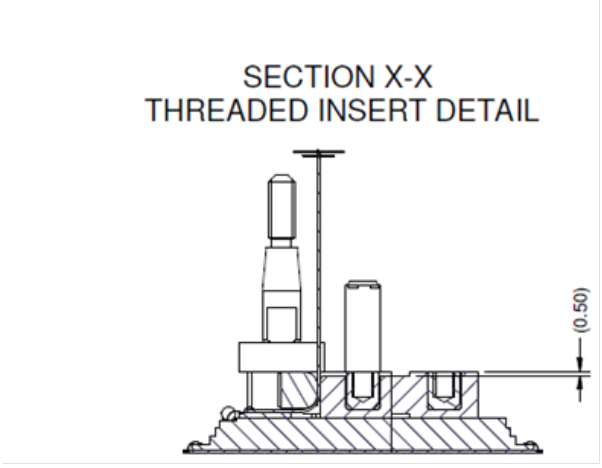
PACKAGE

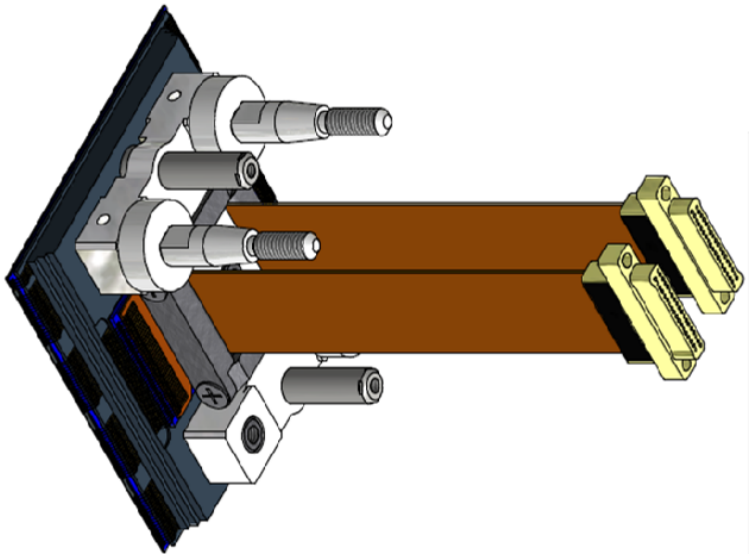
(All dimensions are nominal and are in mm)




6.50
C
29.00
X
B
11.48
20.98
SEE NOTE 1
19.00
A
4.000
SEE NOTE 1
2 x M2x0.4-6H x 6.00 DEEP
X
4.50
SEE NOTE 1
33.00
SEE NOTE 1
2 x M2.5x0.45-6H


A (5 : 1)
PIN 1
PIN 20
PIN 37
PIN 19
PIN1
CONNECTOR A
CONNECTOR B


SECTION X-X
THREADED INSERT DETAIL
(0.50)

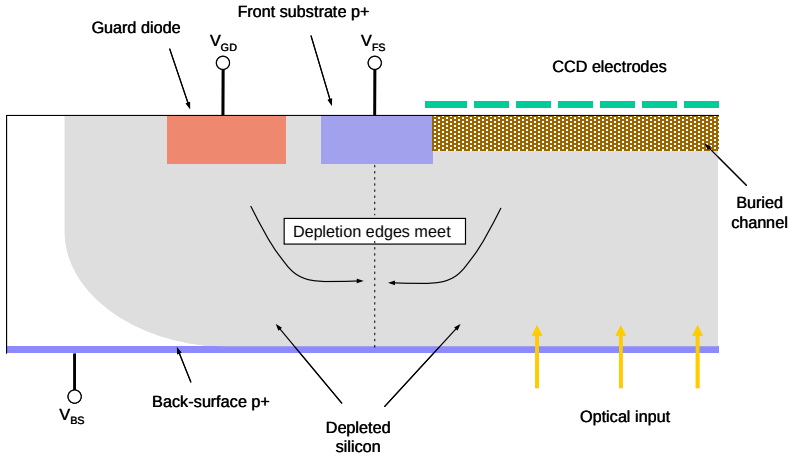


HIGH-RHO DEVICE TECHNOLOGY

Extending the long wavelength response of back-face devices requires the use of thicker silicon, but this must be fully depleted to avoid loss of spatial resolution through sideways diffusion of charge. The depth of depletion is proportional to square root of the operating voltages and the silicon resistivity, but there is a practical limit to both and possibilities for maintaining full-depletion with increasing thickness are therefore limited. The new High-Rho technology is a way of overcoming this limitation.

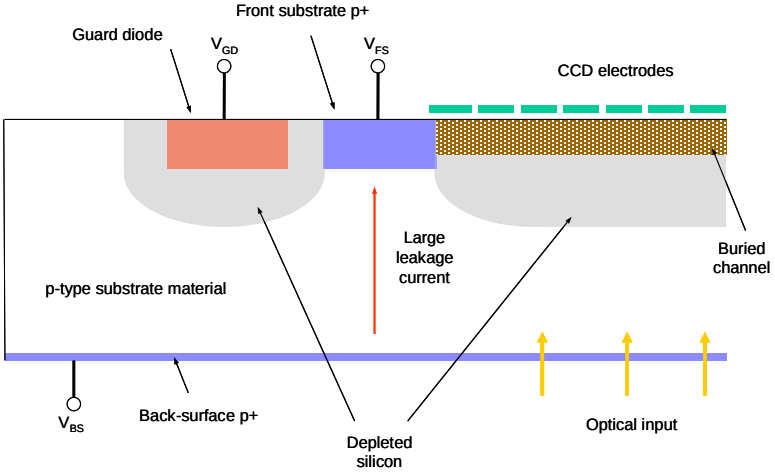
In standard devices the bulk of the silicon substrate is all at the same bias voltage V_{SS}. It is possible to take V_{SS} to negative voltages to increase depletion, but the limit is generally set by the onset of avalanche breakdown in the p-n junctions of the output circuit components.

The High-Rho technology allows the use of a larger negative substrate bias on the back of the silicon V_{BS} to increase the depth of depletion under the electrodes, whilst still maintaining a bias on the front-surface of the silicon V_{FS} at a voltage level normally used for V_{SS} such that the output circuits function normally. However, for this to be possible, current flow between the front and back bias connections must be avoided. This is achieved using an additional “guard diode” at bias V_{GD}, as shown below.



With correct bias conditions the depletion regions from the CCD channel and the guard diode merge to block the conductive path, rather like the operation of a JFET, as shown above. If incorrect, then there is a direct resistive path between the front and back contacts and excessive currents can flow, as shown below.

It is therefore important to use the specified bias levels and the switch-on and switch-off sequences.



ORDERING INFORMATION

CCD250-82-g-xxx
g = cosmetic grade
xxx= specific variant type (e.g. thickness and AR coating)

CCD250-82-g-H08
Enhanced Multi-15 (100 µm thick)

For further information on the performance of this and other options, please contact Teledyne e2v.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:-

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty.

HIGH ENERGY RADIATION

Device characteristics will change when subject to ionising radiation.
Users planning to operate CCDs in high radiation environments are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	148	-	373	K
Operating	148	178	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling ..... 5 K/min