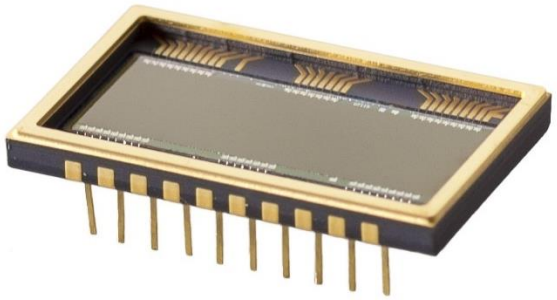
CCD30-11

BSI CCD Sensor



KEY FEATURES

- Back illuminated format for high quantum efficiency.
- Symmetrical Anti-static gate protection
- Anti-blooming readout register
- Deep depletion options for Red/NIR
- Uncoated options for soft X-Ray

TYPICAL APPLICATIONS

- Spectroscopy
- Scientific imaging
- TDI Imaging

PART REFERENCES

Please see last page for full list of available parts

GENERAL DATA

Format	
Image Area	26.6 x 6.67 mm
Active Pixels	1024 (H) x 256 (V)
Pixel Size	26 x 26 µm
Number of Output Amplifiers	1
Package	
Package Size	32.89 x 20.07 mm
Number of Pins	20
Inter-pin Spacing	2.54 mm
Window Material	Removable Glass
Package Type	Ceramic DIL array
Performance (low noise mode)	
Maximum readout frequency	5 MHz
Output Amplifier Sensitivity (NIMO)	2.0 µV/e^-
Output Amplifier Sensitivity (AIMO)	1.5 µV/e^-
Peak Signal (NIMO)	700 ke^-/pixel
Peak Signal (AIMO)	500 ke^-/pixel
Spectral Range	200 - 1060 nm
Readout Noise (NIMO)	5 e^-rms
Readout Noise (AIMO)	6 e^-rms

OVERVIEW

Back illumination technology in combination with high dynamic range makes this device well suited to demanding spectroscopy applications.

The readout register is organised along the long (1024 pixel) edge of the sensor and contains an anti-blooming drain to allow high speed binning operations of low-level signals which may be adjacent to much stronger signals. The novel output amplifier design has no light emission.

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Template: 1B300000-DFP Ver 1
CM 5004004

Approved for public release: Teledyne e2v APPROVED

PERFORMANCE

NIMO

Parameter		Min	Typical	Max	Units	Note
Peak Charge Storage		-	700,000	-	e^-/pixel	1,4
Peak output voltage (unbinned)		-	1.4	-	V	4
Charge transfer efficiency	Parallel	-	99.9999	-	%	3
	Serial	-	99.9993	-		
Output amplifier responsivity		1.3	2.0	2.3	$\mu V/e^-$	-
Readout noise		-	5	8	rms e^-	6
Readout frequency		-	45	5,000	kHz	7
Dark signal at 293K		-	170,000	340,000	e^-/pixel/s	2, 8
Binned column dark signal non-uniformity at 293K (std. deviation)		-	5,000	10,000	e^-/pixel/s	8
Output node capacity		-	1,000,000	-	e^-	-

AIMO

Parameter		Min	Typical	Max	Units	Note
Peak Charge Storage		-	500,000	-	e^-/pixel	1,4
Peak output voltage (unbinned)		-	0.75	-	V	4
Charge transfer efficiency	Parallel	-	99.9999	-	%	3
	Serial	-	99.9993	-		
Output amplifier responsivity		1.3	1.8	2.3	$\mu V/e^-$	-
Readout noise		-	6	8	rms e^-	5
Readout frequency		-	20	5,000	kHz	7
Dark signal at 293K			1,000	2,000	e^-/pixel/s	2, 8
Binned column dark signal non-uniformity at 293K (std. deviation)		-	30	60	e^-/pixel/s	8
Output node capacity		-	1,000,000	-	e^-	-

NOTES

1. Signal level at which resolution begins to degrade. The typical values are those expected from design.
2. The typical average (background) dark signal at any temperature T (kelvin) between 230 K and 300 K is given by:

   NIMO: $Q_d/Q_{d0} = 122T^3e^{-6400/T}$

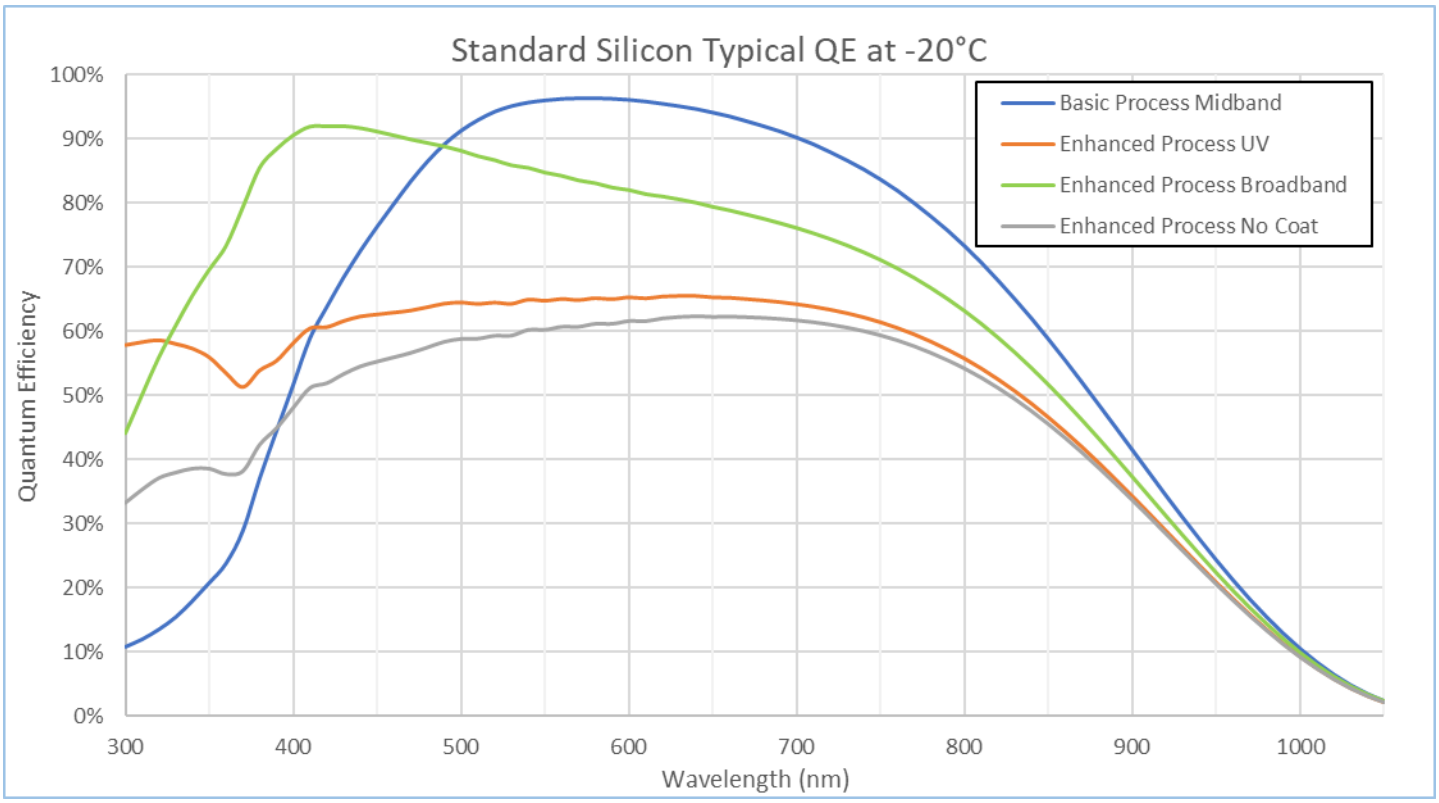
   AIMO: $Q_d/Q_{d0} = 1.14 \times 10^6\ T^3 e^{\ 9080\ /\ T}$

   where Q_{d0} is the dark signal at 293 K. Note that this is typical performance, and some variation may be seen between devices. Below 230 K additional dark current components with a weaker temperature dependence may become significant.
3. CCD Characterisation measurements made using charge generated by X-Ray photons of known energy.
4. Not measured on each sensor but expected to exceed the typical value.
5. Measured using a dual-slope integrator technique (i.e correlated double sampling) with a 10µs integration period.
6. Measured at a pixel readout frequency of 18kHz using dual-slope integrator technique (i.e correlated double sampling). All other tests measured at 45kHz.
7. Readout above 5,000 kHz can be achieved but performance to the parameters given cannot be guaranteed.
8. Dark signal and DSNU values specified at 293K are calculated from tests performed at 243K for NIMO and 273K for AIMO with full parallel binning.
9. QE has a temperature dependence, with lower values as temperature decreased.

SPECTRAL RESPONSE

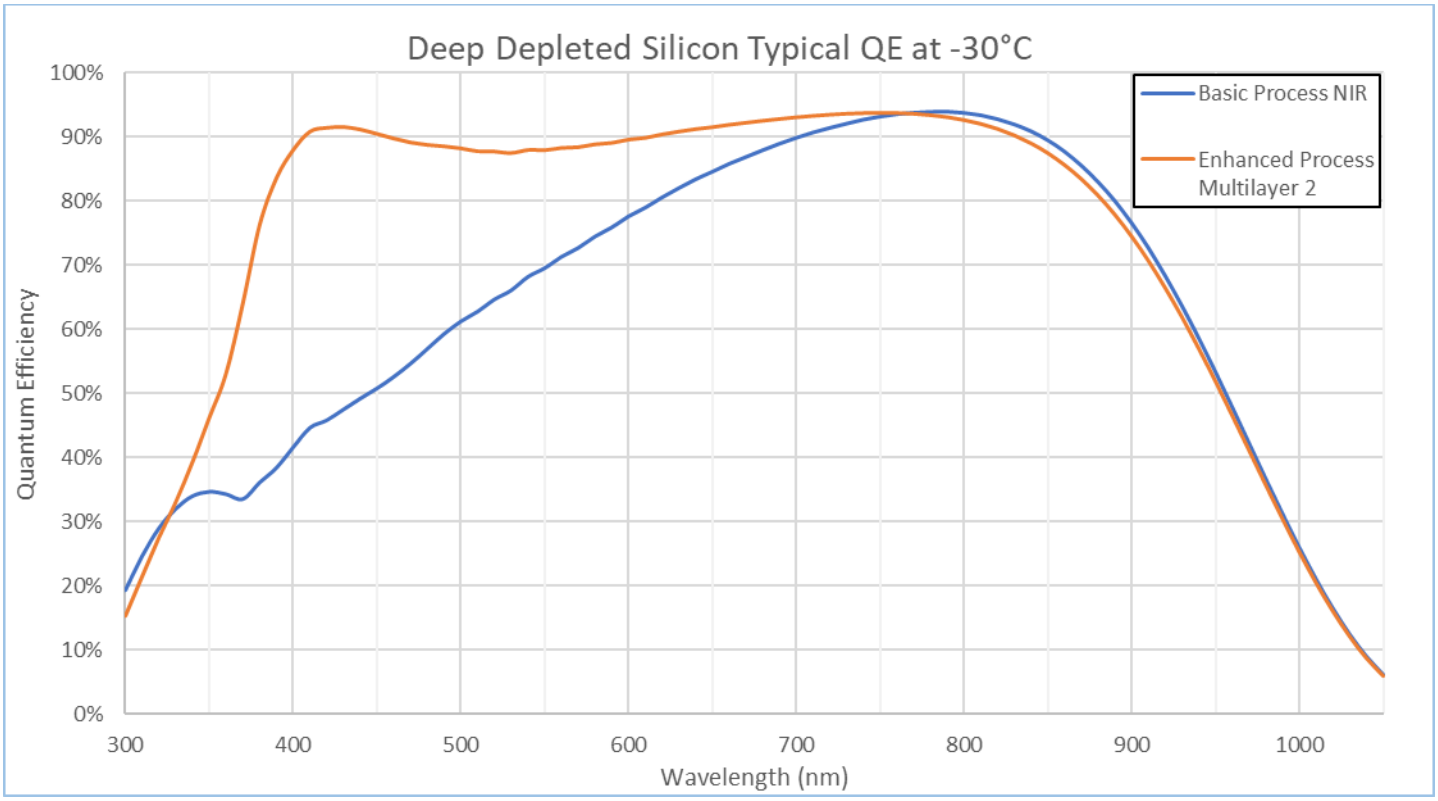
Standard Silicon at -20°C

Wavelength (nm)	Minimum Response (QE) (see note 9)				Maximum Response Non-uniformity (1σ)	
	Enhanced Process UV Coated	Enhanced Process Uncoated	Enhanced Process Broadband coated	Basic Process Midband		
300	45	-	-	-	-	**%**
350	50	20	-	15	-	**%**
400	55	35	80	40	3	**%**
500	60	50	80	85	-	**%**
650	60	50	75	85	3	**%**
900	25	25	25	25	5	**%**



Deep Depleted Silicon at -30°C

Wavelength (nm)	Minimum Response (QE) (see note 9)		Maximum Response Non-uniformity (1σ)	
	Enhanced Process Multilayer 2 Coated	Basic Process NIR Coated		
350	15	30	-	**%**
400	30	75	3	**%**
500	50	75	-	**%**
650	75	80	3	**%**
900	65	65	5	**%**



COSMETIC SPECIFICATION

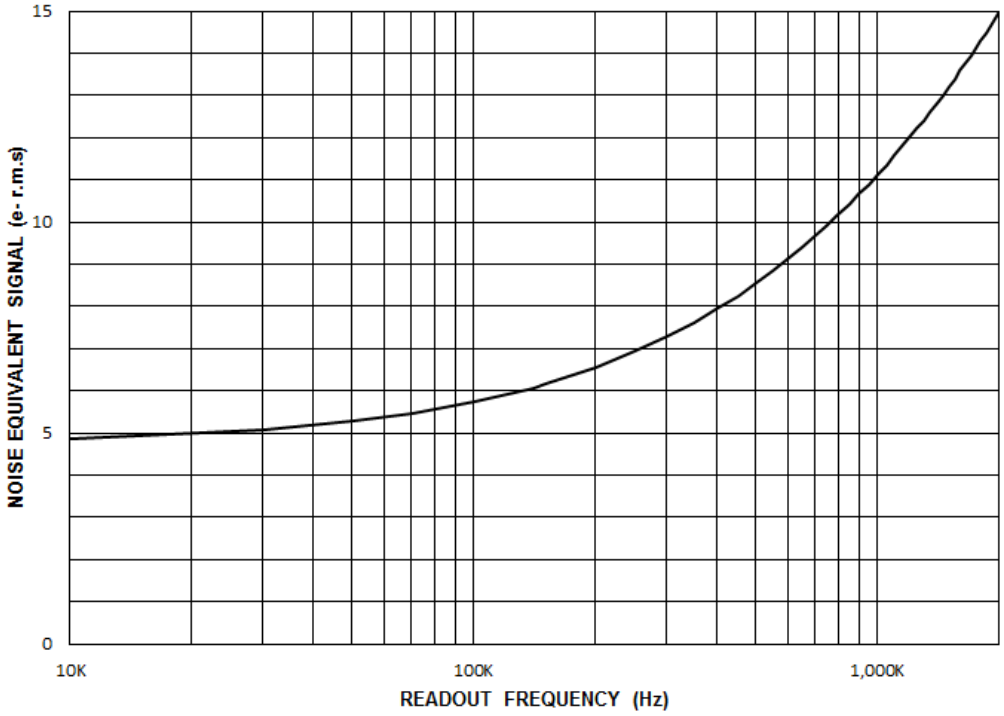
Grade	0	1
Black or Slipped columns	0	2
White columns	0	0
Black spots	12	25
White spots	20	30
Traps >200 e^-	1	2
Level 1 spikes	10	10
Level 2 spikes	2	2

Cosmetic definitions

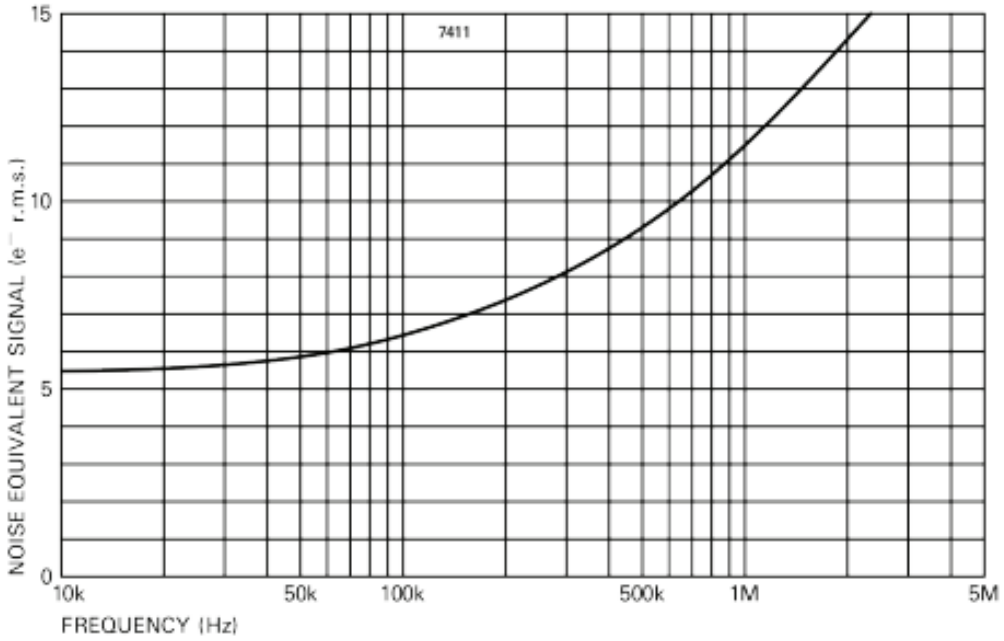
Traps	Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^-. Traps will be observed less at higher temperatures, but more may appear below 233k (NIMO), 243K (AIMO).
Black Spots	Are counted when they have a responsivity of less than 80% of the local mean signal level of approximately half full-well.
White Spots (NIMO)	Are counted when they have a generation rate 8 times the specified maximum dark signal generation rate (measured at 243 K). The amplitude of white spot blemishes decreases rapidly with temperature and is given by: $Q_d/Q_{d0} = 122T^3e^{-6400/T}$
White Spots (AIMO)	Are counted when they have a generation rate 100 times the specified maximum dark signal generation rate (measured between at 233 K and 273 K). The amplitude of white spot blemishes decreases rapidly with temperature and is given by: $Q_d/Q_{d0} = 122T^3e^{-6400/T}$
Column Defects	A column defect which contains at least 9 white or 9 black defects.
Slipped Columns	Are counted if they have an amplitude greater than 200 e^-.
Spikes	Are measured with the image fully binned into the register. Level 1 spikes are column with 6.4 Me-/col or greater equivalent signal at +20°C. Level 2 spikes are columns with 25.6 Me-/col or greater.

TYPICAL OUTPUT CIRCUIT NOISE

NIMO

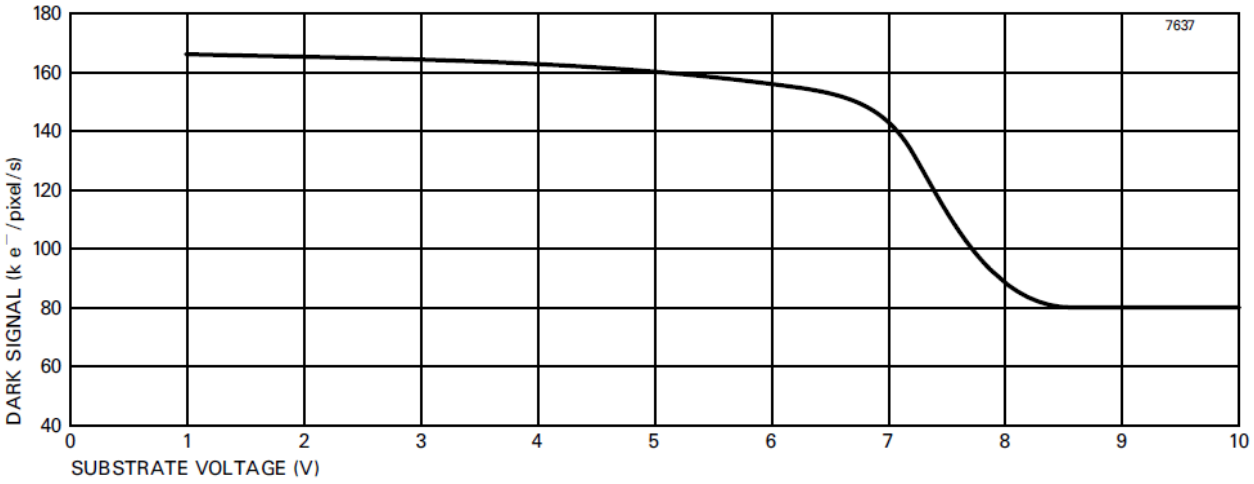


AIMO

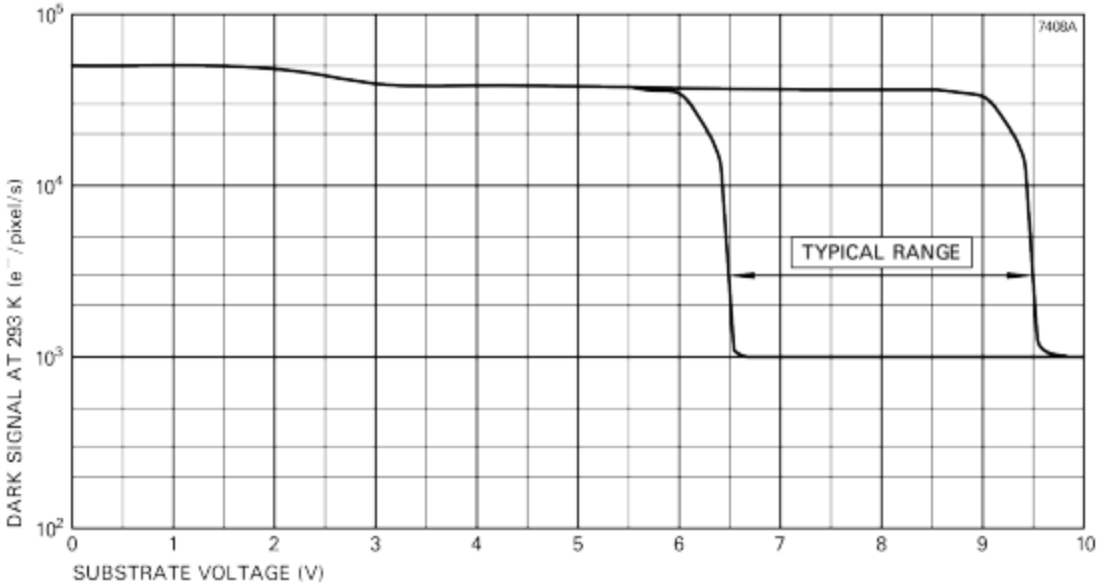


TYPICAL VARIATION OF DARK CURRENT WITH SUBSTRATE VOLTAGE

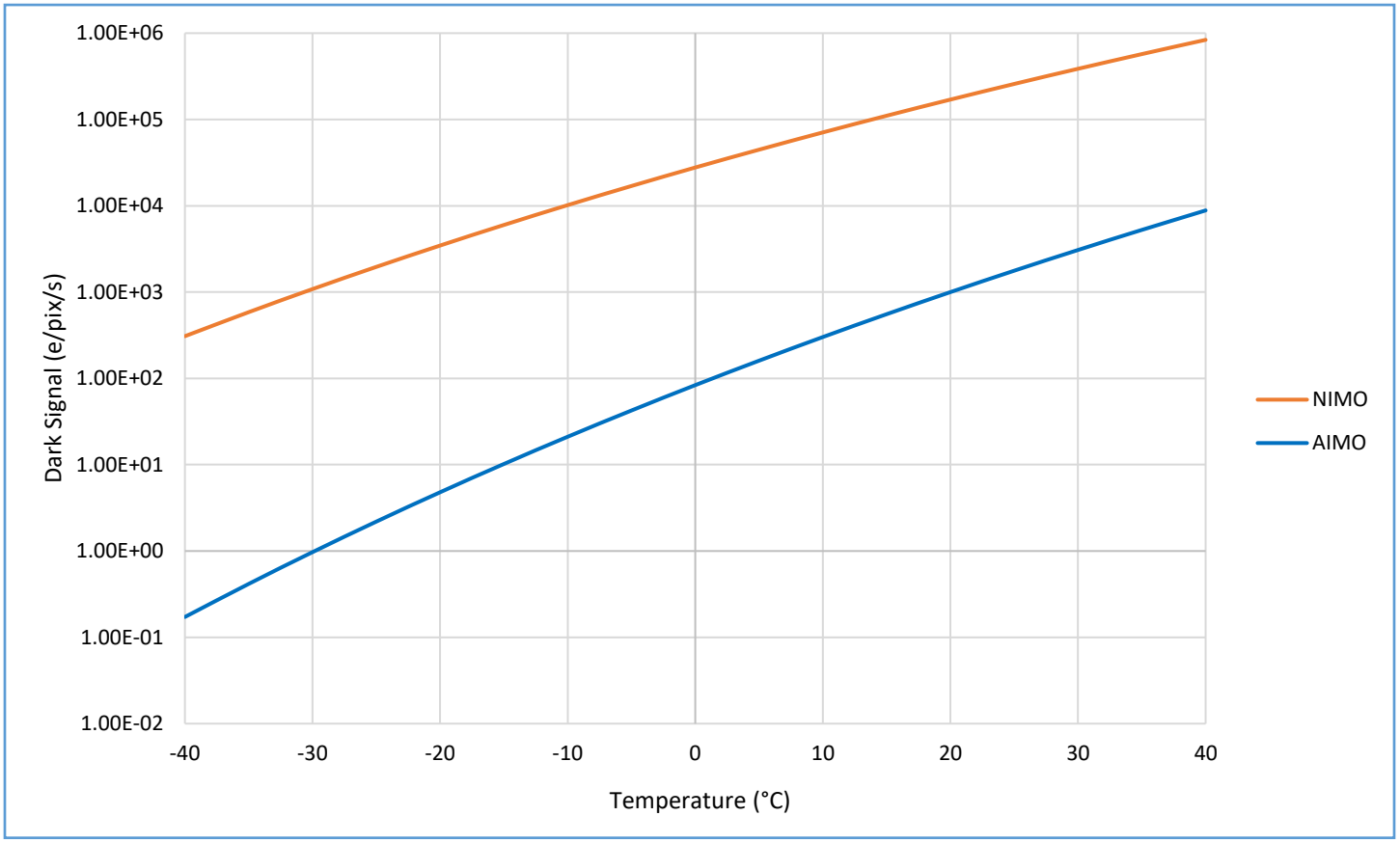
NIMO



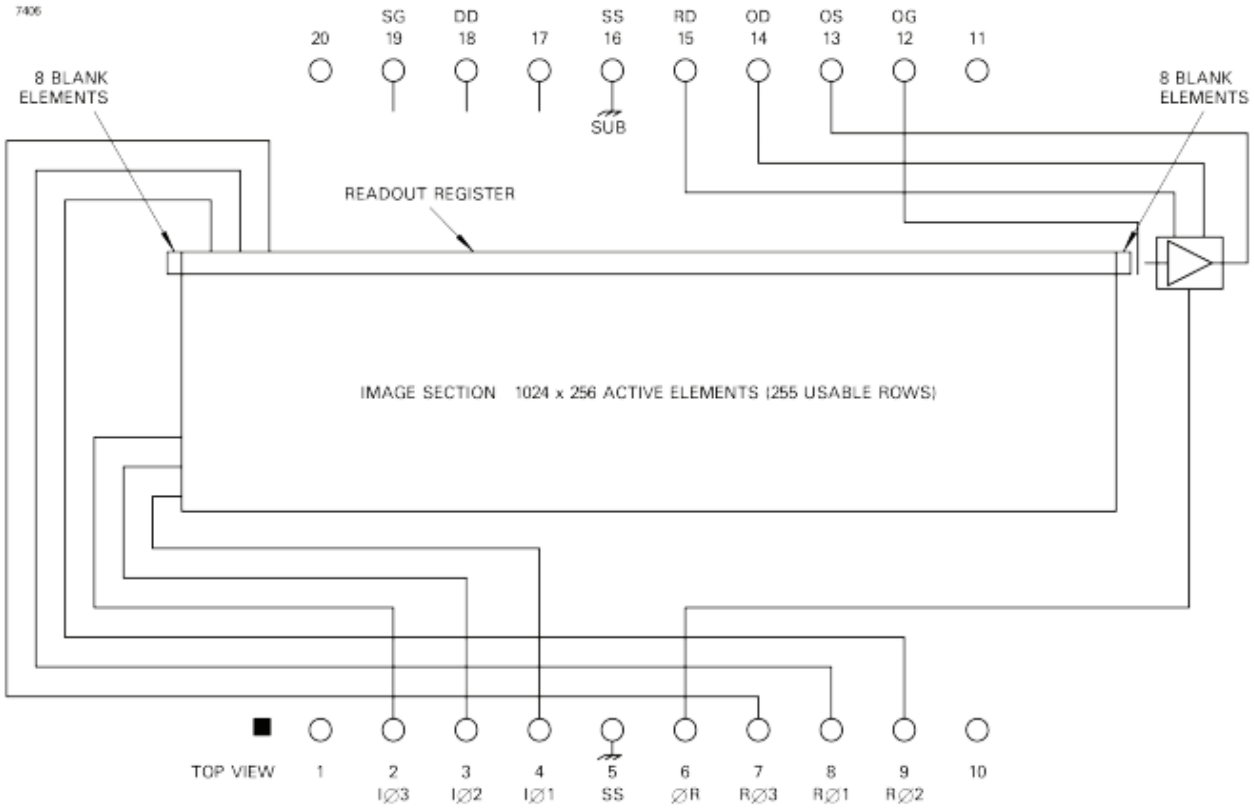
AIMO



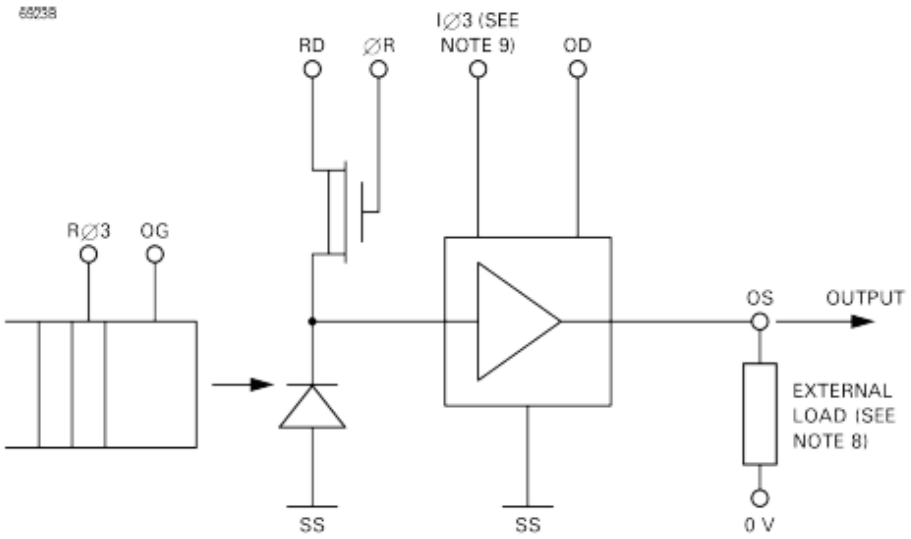
TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE



DEVICE SCHEMATIC



OUTPUT CIRCUIT



NOTES

10. Not critical; can be a 1-5 mA constant current source, or 5-10kΩ resistor.
11. The amplifier has a DC restoration circuit, which is activated internally whenever 1Ø3 is pulsed high.
12. Image selection pulse low levels 0 ± 0.5V; other pulse low levels IØ low +1 V.
13. Output node capacity is typically 2 times that of the image section.
14. There are no temperature sensing diodes in the back thinned version of the CCD30-11.

CONNECTIONS TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

NIMO

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 12)			MAX RATINGS with respect to Vss
			Min	Typical	Max	
1	-	No connection		-		-
2	IØ3	Image section, phase 3 (clock pulse)	8	12	15	±20V
3	IØ2	Image section, phase 2 (clock pulse)	8	12	15	±20V
4	IØ1	Image section, phase 1 (clock pulse)	8	12	15	±20V
5	SS	Substrate	0	3	10	-
6	ØR	Output reset pulse	8	12	15	±20V
7	RØ3	Reset register, phase 3 (clock pulse)	8	11	15	±20V
8	RØ1	Reset register, phase 2 (clock pulse)	8	11	15	±20V
9	RØ2	Reset register, phase 1 (clock pulse)	8	11	15	±20V
10	-	No connection				-
11	-	No connection				-
12	OG	Output gate	1	3	5	±20V
13	OS	Output transistor source		See note 10		-0.3 to +25V
14	OD	Output drain	27	29	32	-0.3 to +32V
15	RD	Reset transistor drain	15	17	19	-0.3 to +25V
16	SS	Substrate	0	3	10	-
17	-	No connection		-		-
18	DD	Dump drain	20	24	25	-0.3 to +25V
19	SG	Spare gate	0	0	VSS +19	±20V
20	-	No connection		-		-

AIMO

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 12)			MAX RATINGS with respect to Vss
			Min	Typical	Max	
1	-	No connection		-		-
2	IØ3	Image section, phase 3 (clock pulse)	8	12	15	±20V
3	IØ2	Image section, phase 2 (clock pulse)	8	12	15	±20V
4	IØ1	Image section, phase 1 (clock pulse)	8	12	15	±20V
5	SS	Substrate	8	9.5	11	-
6	ØR	Output reset pulse	8	12	15	±20V
7	RØ3	Reset register, phase 3 (clock pulse)	8	11	15	±20V
8	RØ1	Reset register, phase 2 (clock pulse)	8	11	15	±20V
9	RØ2	Reset register, phase 1 (clock pulse)	8	11	15	±20V
10	-	No connection		see note 14		-
11	-	No connection		see note 14		-
12	OG	Output gate	1	3	5	±20V
13	OS	Output transistor source		see note 10		-0.3 to +25V
14	OD	Output drain	27	29	32	-0.3 to +25V
15	RD	Reset transistor drain	15	17	19	-0.3 to +25V
16	SS	Substrate	8	9.5	11	-
17	-	No connection		-		-
18	DD	Dump drain	22	24	25	-0.3 to +25V
19	SG	Spare gate	0	0	Vss + 19	±20V
20	-	No connection		-		-

If all voltages are set to the ‘typical’ values, operation at or close to specification should be obtained. Some adjustment within the minimum – maximum range specified may be required to optimise performance.

Voltage between pairs of pins: OS to OD + 15 V. Maximum current through any source or drain pin: 10 mA.

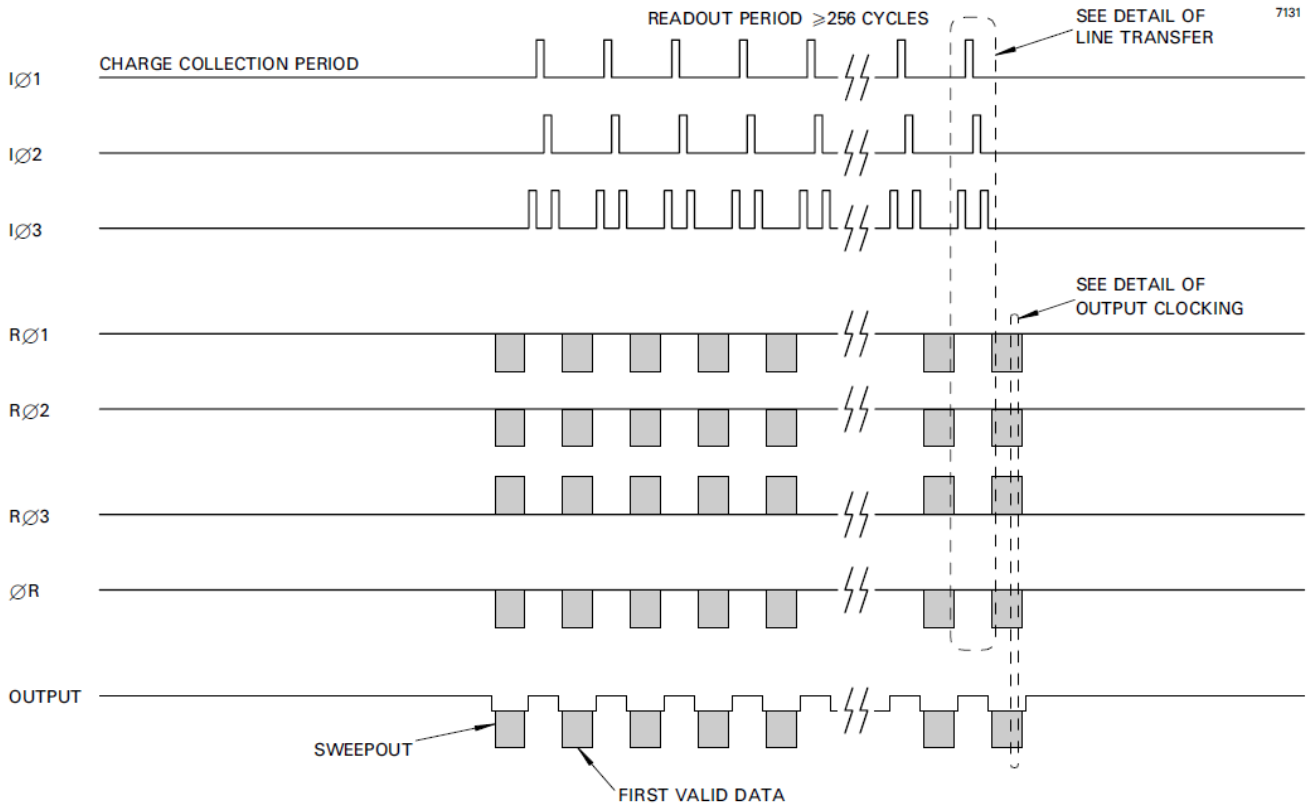
DD controls the anti-blooming function of the register and also biases the drains around the edge of the CCD, protecting the image and register from charge generated elsewhere spilling into these sensitive regions of the device.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode Capacitances (Measured at mid-clock level)

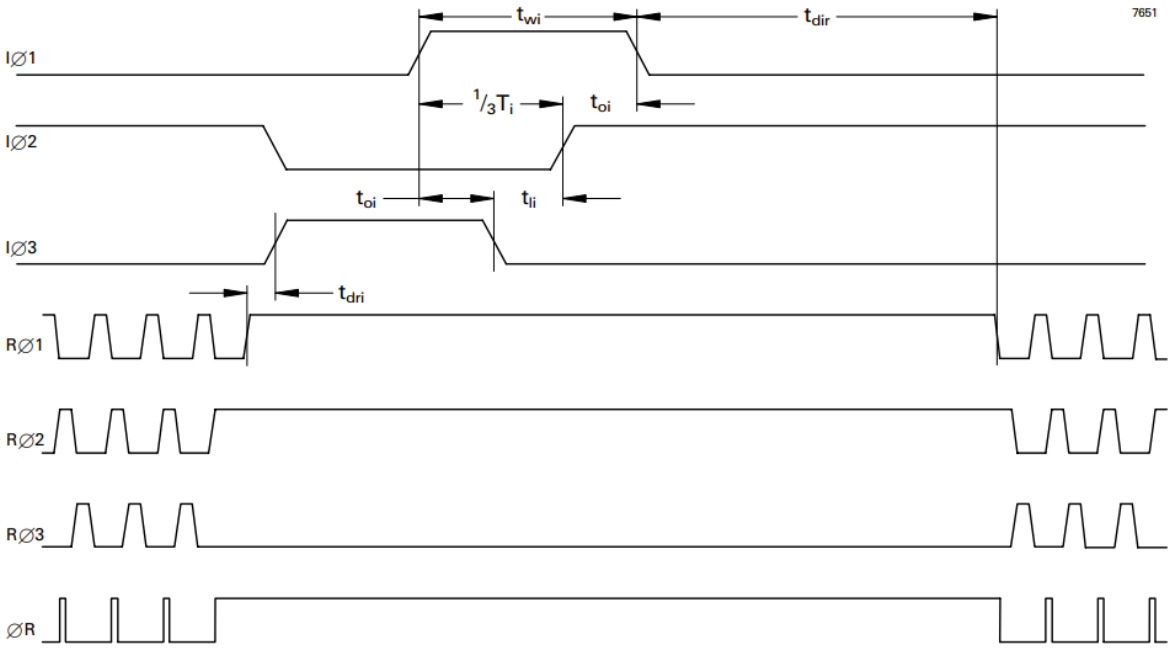
	Typical	
IØ/IØ interphase	2.0	nF
IØ/SS	11	nF
RØ/RØ interphase	70	pF
RØ/(SS + DG + OD)	185	pF
Output impedance	300	Ω

FRAME READOUT TIMING DIAGRAM



DETAIL OF LINE TRANSFER (not to scale)

NIMO



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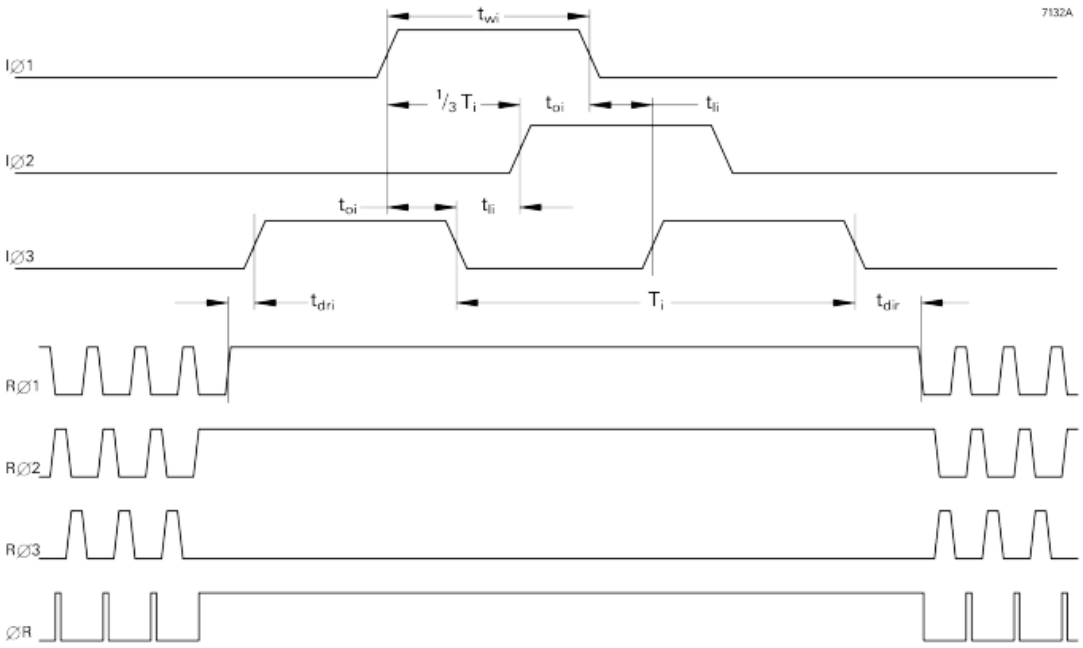
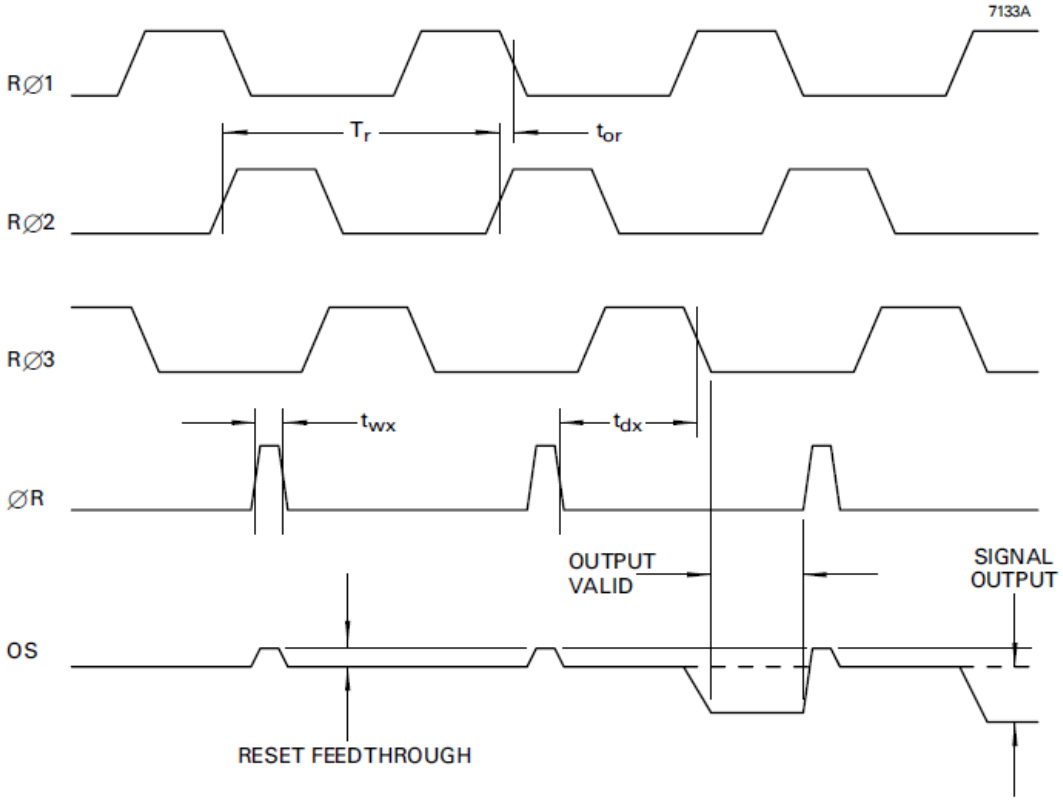
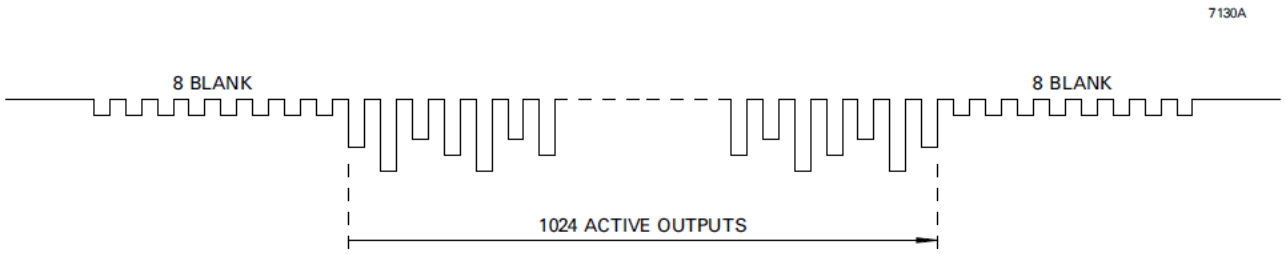


DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



CLOCK TIMING REQUIREMENTS

NIMO

Symbol	Description	Min	Typical	Max	Unit
T_i	Image clock period	10	20	See note 15	µs
t_{wi}	Image clock pulse width	5	10	See note 15	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.5	1	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	1	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	1	2	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	1	5	$0.2T_i$	µs
t_{dir}	Delay time, IØ stop to RØ start	3	10	See note 15	µs
t_{dri}	Delay time, RØ stop to IØ start	1	2	See note 15	µs
T_r	Output register clock cycle period	200	See note 16	See note 15	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.2T_r$	ns
t_{rx} , t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

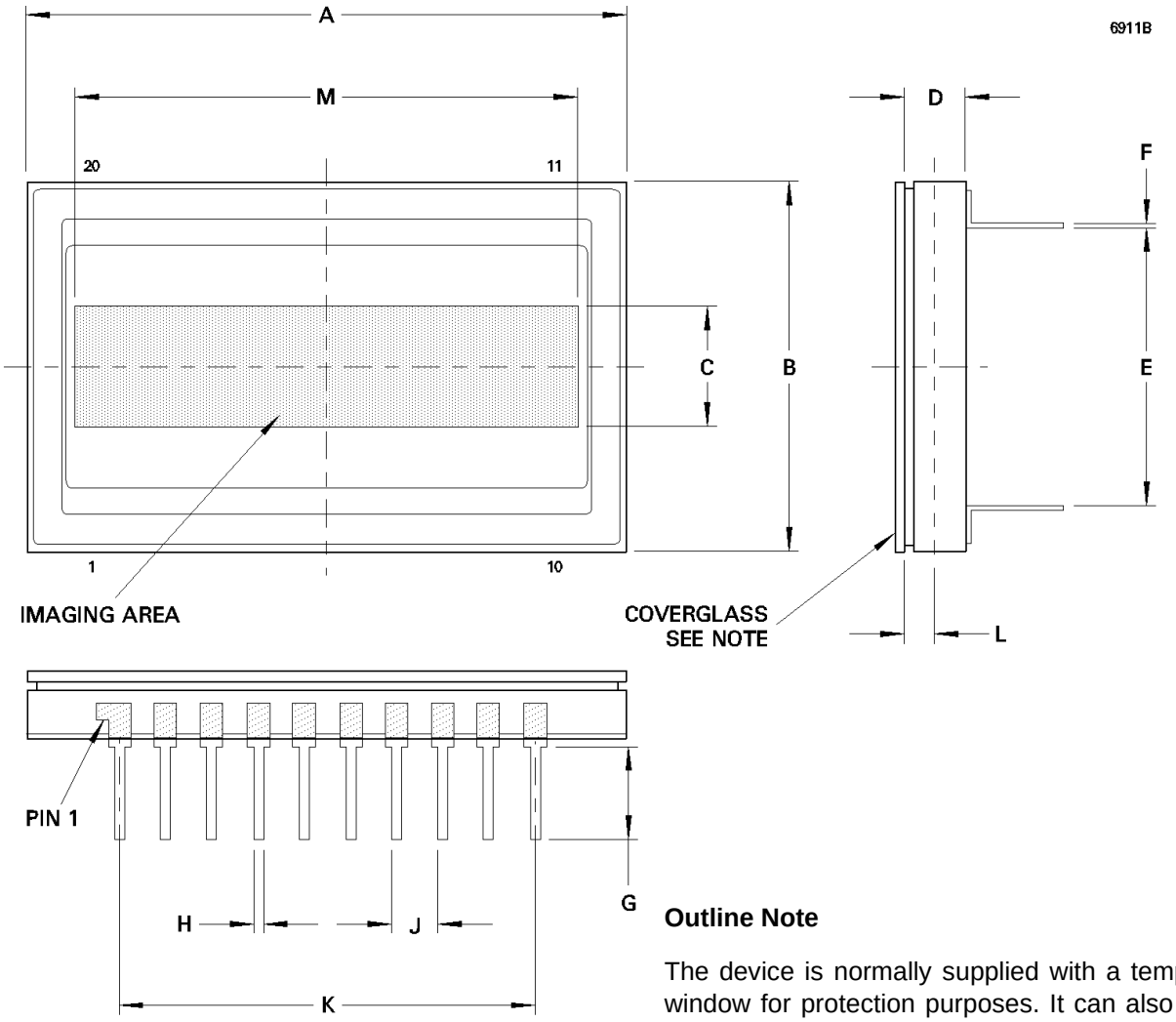
AIMO

Symbol	Description	Min	Typical	Max	Unit
T_i	Image clock period	15	30	see note 15	µs
t_{wi}	Image clock pulse width	7	15	see note 15	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.5	2	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t,;	2	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	3	5	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	3	5	$0.2T_i$	µs
t_{dir}	Delay time, IØ stop to RØ start	3	5	see note 15	µs
t_{dri}	Delay time, RØ stop to IØ start	1	2	see note 15	µs
T_r	Output register clock cycle period	200	see note 16	see note 15	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	0.1T,	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	trr	0.1T,	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	0.5trr	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	0.1T,	$0.2T_r$	ns
t_{rx} , t_{fx}	Reset pulse rise and fall times	20	0.5trr	$0.2T_r$	ns

NOTES

15. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
16. As set by the readout period.

OUTLINE (All dimensions in millimeters; dimensions without limits are nominal)



Outline Note

The device is normally supplied with a temporary glass window for protection purposes. It can also be supplied with a fixed, quartz or fibre-optic window where required.

Ref	Millimeters	
A	32.89 ± 0.38	
B	20.07 ± 0.25	
C	6.7	
D	3.30 ± 0.33	
E	15.24 ± 0.25	
F	0.254	+ 0.051
		- 0.025
G	5.21	
H	0.46 ± 0.05	
J	2.54 ± 0.13	
K	22.86 ± 0.13	
L	1.65 ± 0.56	
M	26.6	

HEALTH AND SAFETY HAZARDS

Teledyne e2v devices are safe to handle and operate, provided that the relevant precautions stated herein are observed. Teledyne e2v does not accept responsibility for damage or injury resulting from the use of devices it produces. Equipment manufacturers and users must ensure that adequate precautions are taken. Appropriate warning labels and notices must be provided on equipment incorporating Teledyne e2v devices and in operating manuals.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising radiation. Users planning to use CCDs in a high radiation environment are advised to contact Teledyne e2v. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 3, 4, 6, 7, 8, 9, 12, 19) but not to the other pins.

TEMPERATURE LIMITS

	Min	Typical	Max
Storage	73	-	373 K
Operating	73	233	323 K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling ..... 5 K/min

PART REFERENCES

Variant	Operating Mode	Illumination	Enhanced BSI Process	Silicon	AR Coating	Fringe Suppression
CCD30-11-G-182	AIMO	BSI	No	Standard	Midband	Yes
CCD30-11-G-311	AIMO	BSI	Yes	Standard	UV	No
CCD30-11-G-315	AIMO	BSI	Yes	Standard	Broadband	No
CCD30-11-G-971	AIMO	BSI	No	Standard	Midband	No
CCD30-11-G-973	AIMO	BSI	Yes	Standard	None	No
CCD30-11-G-196	NIMO	BSI	Yes	Deep Depleted	Multi-2	Yes
CCD30-11-G-387	NIMO	BSI	No	Deep Depleted	NIR	Yes

Grade Definitions

Grade 0	Super Grade	Meets all performance parameters and Grade 0 cosmetic parameters
Grade 1	Science Grade	Meets all performance parameters and Grade 1 cosmetic parameters
Grade 5	Engineering Grade	Electrically functional with no performance or cosmetic parameter guarantees
Grade 6	Mechanical Grade	Non-functional. Mechanically representative only.

NOTES

17. G = Grade (e.g. 1)
18. Additional variants may be available to custom order. Consult Teledyne e2v for more information.