CCD30–11 Front Illuminated Open Electrode High Performance CCD Sensor

FEATURES

- 1024 by 256 Pixel Format
- 26 µm Square Pixels
- Image Area 26.6 x 6.7 mm
- Wide Dynamic Range
- Symmetrical Anti-static Gate Protection
- Open Electrode Structure for Enhanced Quantum Efficiency
- Advanced Inverted Mode Operation
- Anti-blooming Readout Register
- Zero Light Emitting Output Amplifier.

APPLICATIONS

- Spectroscopy
- Scientific Imaging
- TDI Operation.

INTRODUCTION

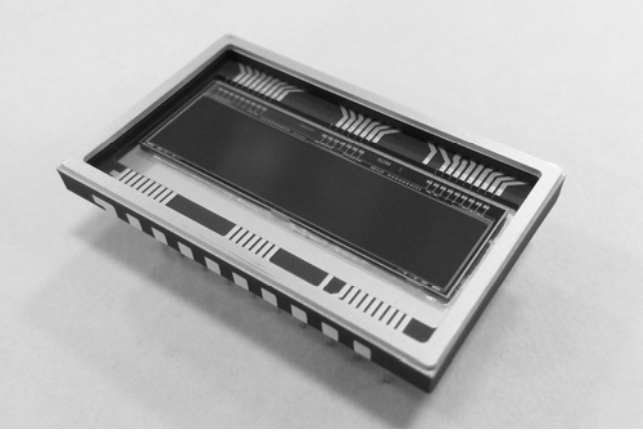
The open electrode CCD30-11 is a high performance CCD sensor designed as an upgrade for the standard CCD30-11, for use in the scientific spectroscopy instrument market, where enhanced quantum efficiency is required at near-ultraviolet wavelengths. With an array of 1024 x 256 26 µm square pixels it has an imaging area to suit most spectrometer outputs of 26.6 x 6.7 mm (1.05 x 0.26 inch).

The readout register is organised along the long (1024 pixel) edge of the sensor and contains an anti-blooming drain to allow high speed binning operations of low level signals which may be adjacent to much stronger signals. The novel output amplifier design has no light emission.

Standard three phase clocking and buried channel charge transfer are employed and Advanced Inverted Mode Operation (AIMO) is included as standard.

The open electrode CCD30-11 is packaged in a 20-pin DIL ceramic package and is pin compatible (but not completely clock compatible) with the standard CCD30-11.

Designers are advised to consult e2v technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging.



TYPICAL PERFORMANCE

Pixel readout frequency	45 kHz
Output amplifier sensitivity	1.8 µV/e^-
Peak signal	300 ke^-/pixel
Dynamic range	75000:1
Spectral range	200 – 1060 nm
Readout noise	4 e^- rms
QE at 700nm	50 %
Peak output voltage	540 mV

GENERAL DATA

Format

Image area	26.6 x 6.7 mm
Active pixels	1024 (H) x 256 (V)
Pixel size	26 x 26 µm

Package

Package size	32.89 x 20.07 mm
Number of pins	20
Inter-pin spacing	2.54 mm
Inter-row spacing	15.24 mm
Window material	quartz or removable glass

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PERFORMANCE

		Min	Typical	Max	Units	Note
Peak charge storage			300,000		e^-/pixel	1
Peak output voltage (unbinned)			540		mV	1
Dark signal at 293 K			250	500	e^-/pixel/s	2, 6
Charge transfer efficiency	Parallel		>99.999		%	3
	Serial		>99.999		%	
Output amplifier sensitivity		1.3	1.8	2.3	µV/e^-	
Readout noise at 253 K			4	6	rms e^-/pixel	4
Readout frequency			45	5000	kHz	5
Photo response non-uniformity (std. deviation)			3		% of mean	
Binned column dark signal non-uniformity at 293 K (std. deviation)				15	e^-/pixel/s	6
Binned column DSNU spikes at 293 K	No. of columns >50 ke^-/s			10		6
	No. of columns >200 ke^-/s			2		6

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (at mid-clock level):

	Typical	Units
IØ/IØ interphase	2.0	nF
RØ/RØ interphase	70	pF
IØ/SS	11	nF
RØ/SS	185	pF
Output impedance	300	Ω

NOTES

1. Signal level at which resolution begins to degrade. The typical values are those expected from design.
2. The typical average (background) dark signal at any temperature T (kelvin) between 230 and 300 K is given by:
$$Q_d/Q_{d0} = 1.14 \times 10^6 T^3 e^{-9080/T}$$
where Q_{d0} is the dark current at 293 K. Note that this is typical performance and some variation may be seen between devices. Below 230 K additional dark current components with a weaker temperature dependence may become significant.
3. Not routinely measured but expected to exceed the typical value.
4. Measured at a pixel readout frequency of 18 KHz using a dual-slope integrator technique (i.e. correlated double sampling). All other tests measured at 45 kHz.
5. Readout above 5000 kHz can be achieved but performance to the parameters given cannot be guaranteed.
6. Dark signal and DSNU values specified at 293 K are calculated from tests performed at 273 K.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps can be seen as a line of trailing charge.

Black spots Are counted when they have a responsivity outside 10% of the local mean signal.

White column A column which contains at least 9 white defects.

Black column A column which contains at least 9 black defects.

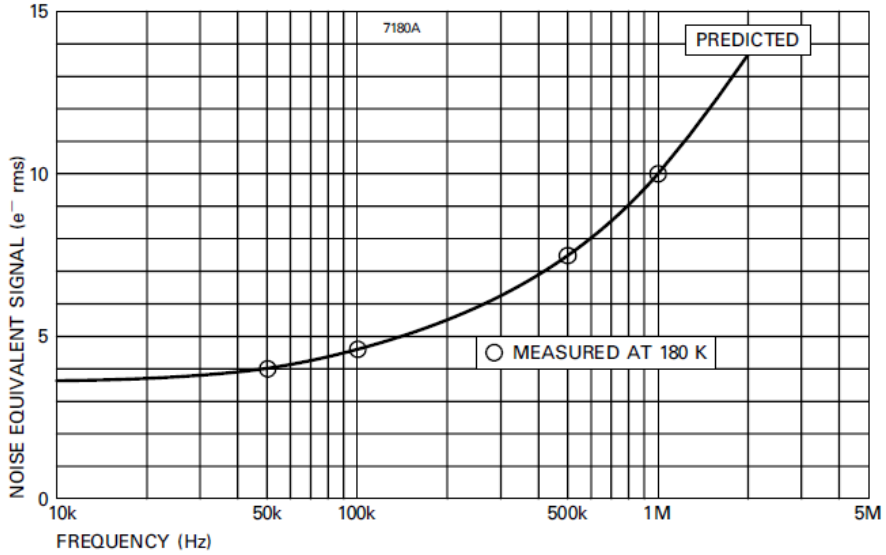
White spots Are counted when they have a generation rate 40 times the specified maximum dark signal generation rate at 293 K. The typical temperature dependence of white spot blemishes is different from that of the average dark signal and is given by:
$$Q_d/Q_{d0} = 122T^3 e^{-6400/T}$$

GRADE	**0**	**1**	**2**
Column defects: black	0	1	6
white	0	0	0
Black spots	9	16	80
Traps	1	2	5
White spots	10	10	15

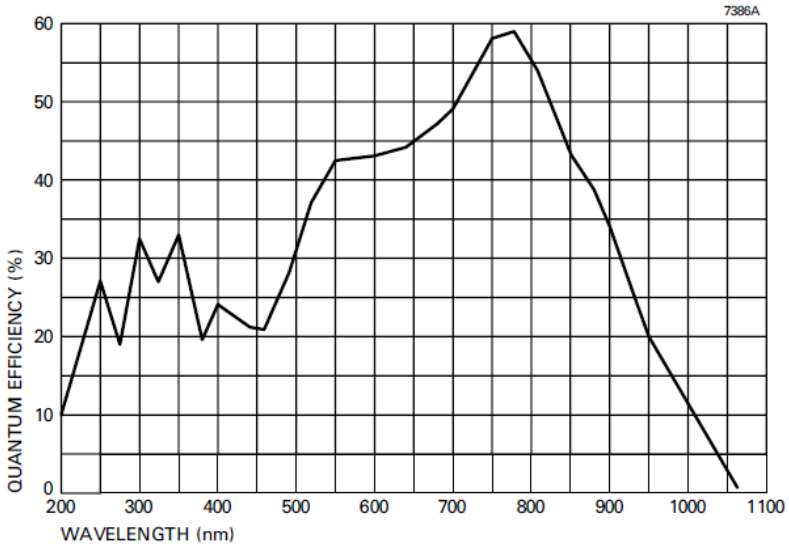
Minimum separation between adjacent black columns ..... 50 pixels

Note The amplitude of white spots and columns will decrease rapidly with temperature.

TYPICAL OUTPUT CIRCUIT NOISE (If measured using clamp and sample)



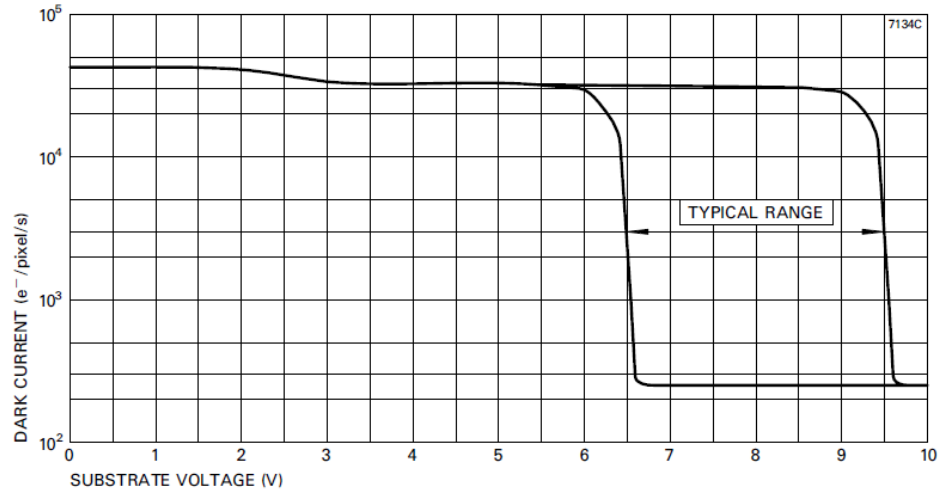
TYPICAL SPECTRAL RESPONSE (No window)



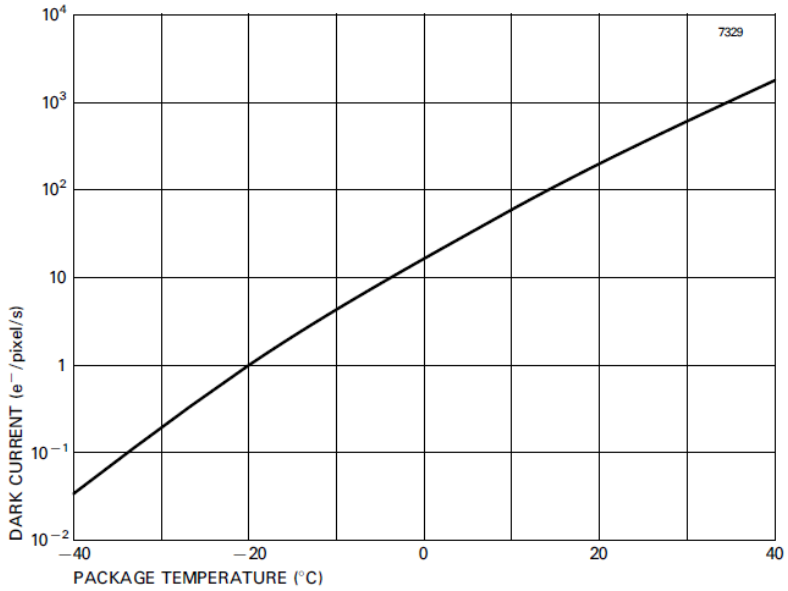
NOTE

7. Quantum Efficiency is not measured during factory tests. See technical paper on the e2v website titled “UV Conversion Coatings”.

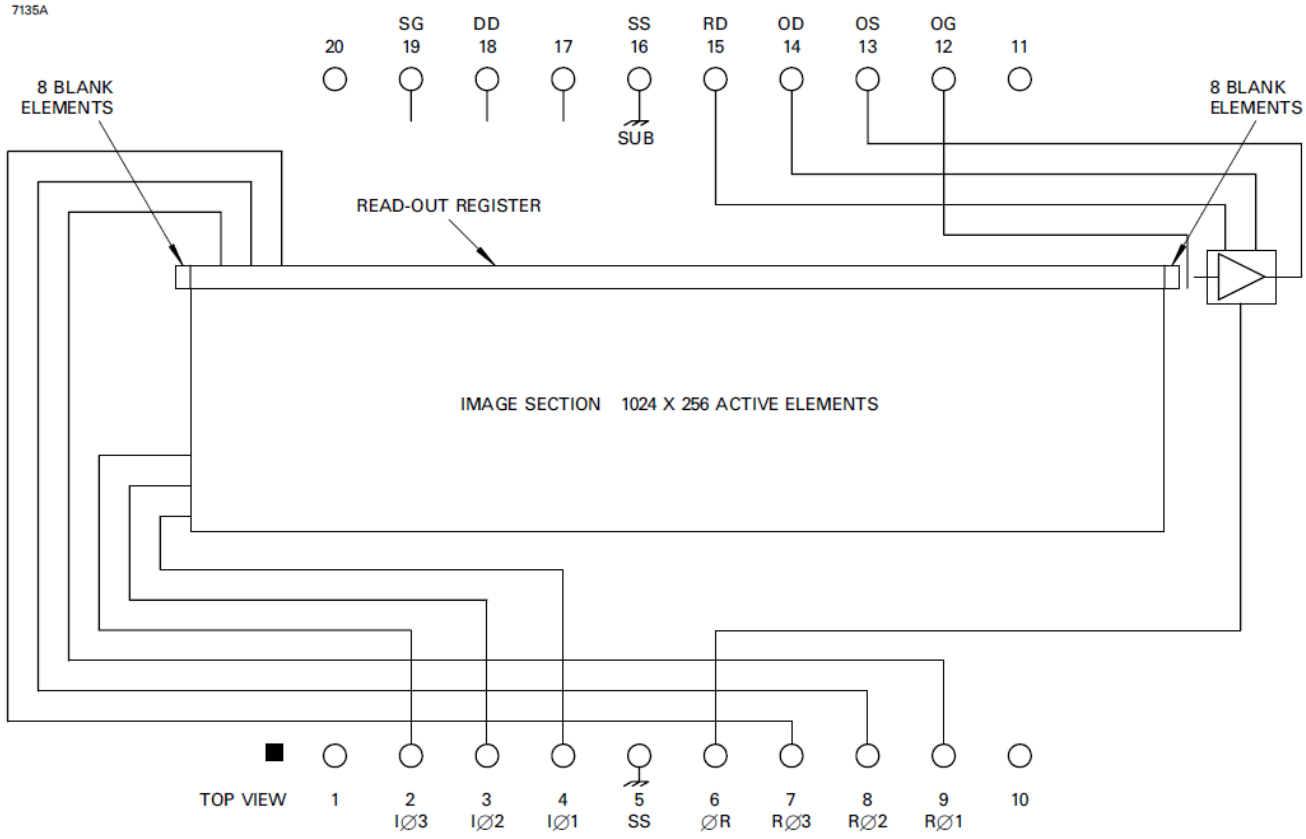
TYPICAL VARIATION OF DARK CURRENT WITH SUBSTRATE VOLTAGE



TYPICAL VARIATION OF DARK CURRENT WITH TEMPERATURE



DEVICE SCHEMATIC

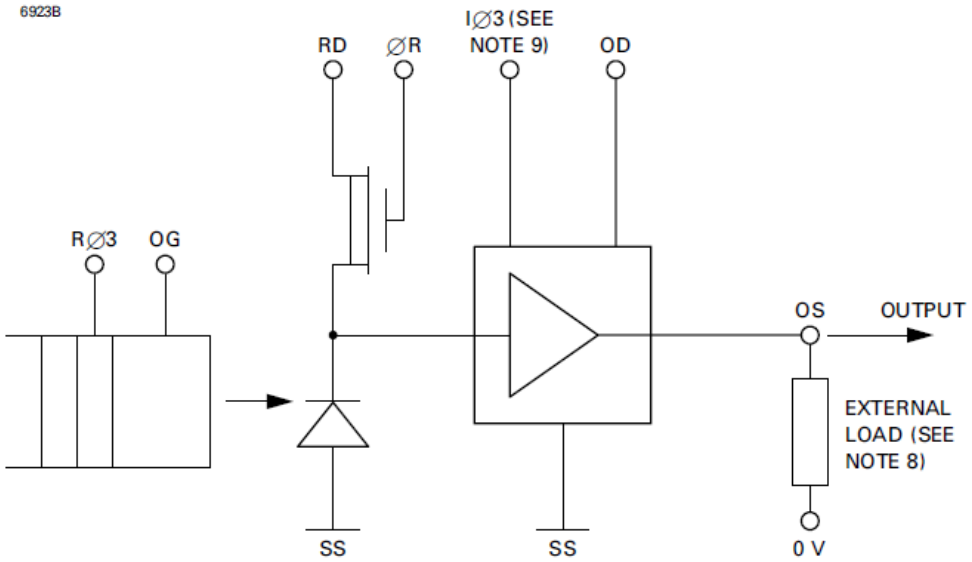


CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 10)			MAX RATINGS with respect to Substrate SS
			Min	Typical	Max	
1	-	No connection		-		-
2	IØ3	Image section, phase 3 (clock pulse)	10	12	15	±20 V
3	IØ2	Image section, phase 2 (clock pulse)	10	12	15	±20 V
4	IØ1	Image section, phase 1 (clock pulse)	10	12	15	±20 V
5	SS	Substrate	8	8.5	11	-
6	ØR	Output reset pulse	10	12	15	±20 V
7	RØ3	Reset register, phase 3 (clock pulse)	10	12	15	±20 V
8	RØ2	Reset register, phase 2 (clock pulse)	10	12	15	±20 V
9	RØ1	Reset register, phase 1 (clock pulse)	10	12	15	±20 V
10	-	No connection				-
11	-	No connection				-
12	OG	Output gate	2	3.5	5	±20 V
13	OS	Output transistor source		See note 8		-0.3 to +25 V
14	OD	Output drain	27	30	31	-0.3 to +25 V
15	RD	Reset transistor drain	17	18	19	-0.3 to +25 V
16	SS	Substrate	8	8.5	11	-0.3 to +25 V
17	-	No connection		-		-
18	DD	Dump drain	20	22	25	-0.3 to +25 V
19	SG	Spare gate	0	0	V_{SS} +19	±20 V
20	-	No connection		-		-

If all voltages are set to the 'typical' values, operation at or close to typical specification should be obtained. Some adjustment within the minimum – maximum range specified may be required to optimise performance.
Voltage between pairs of pins: OS to OD + 15 V. Maximum current through any source or drain pin: 10 mA.
SG needs to be grounded to prevent unwanted charge moving into the register.
DD controls the anti blooming function of the register and also biases the drains around the edge of the CCD, protecting the image and register from charge generated elsewhere spilling into these sensitive regions of the device.

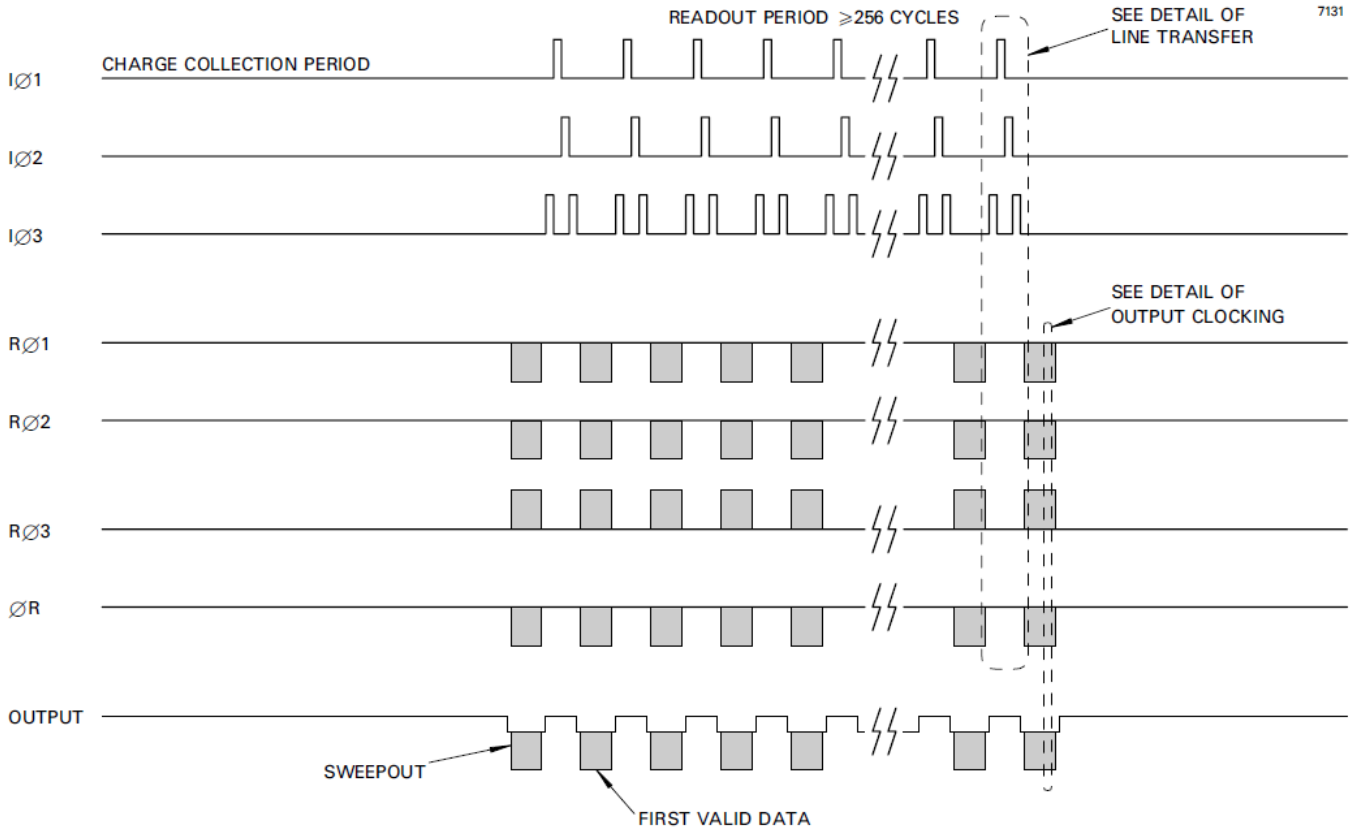
OUTPUT CIRCUIT



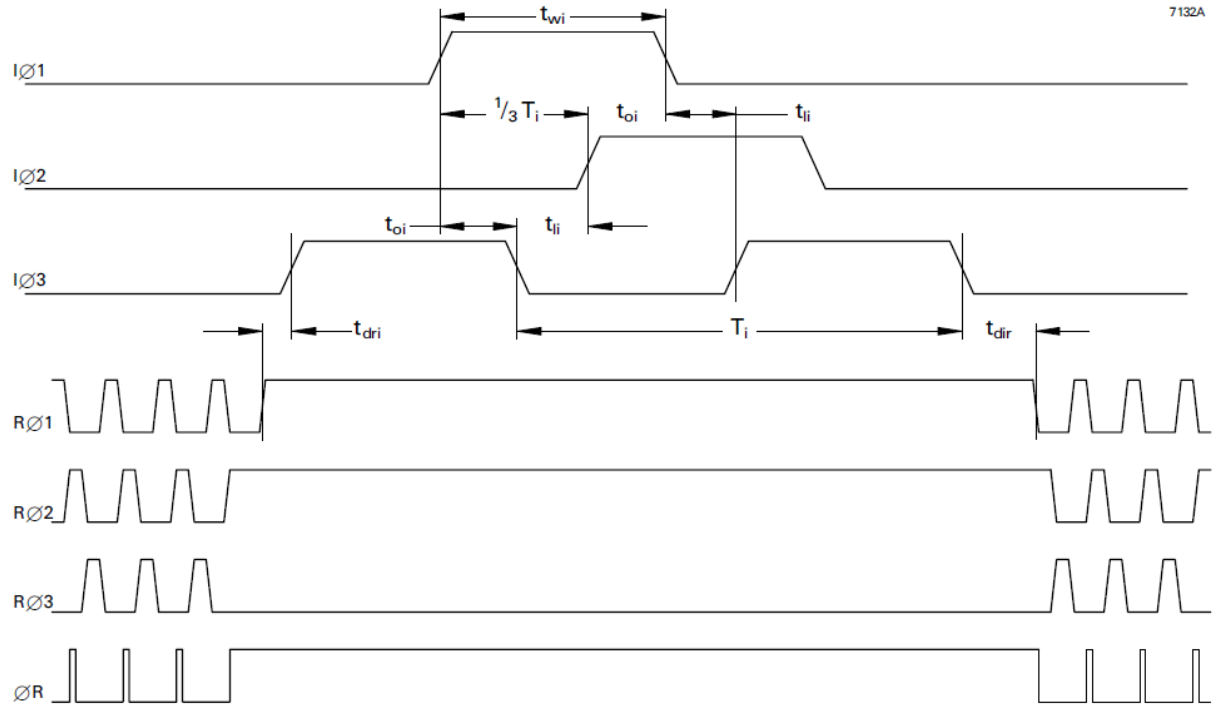
NOTES

8. Not critical; can be a 1 – 5 mA constant current source, or 5 – 10 kΩ resistor.
9. The amplifier has a DC restoration circuit, which is activated internally whenever IØ3 is pulsed high.
10. All pulse low levels 0 ± 0.5 V.
11. Output node capacity is typically 4 times that of the image section.

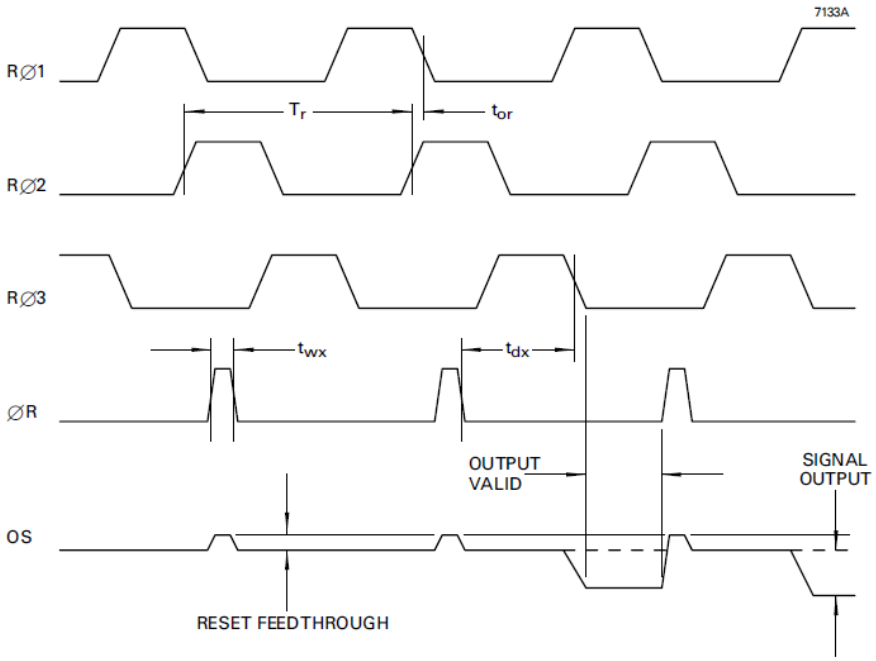
FRAME READOUT TIMING DIAGRAM



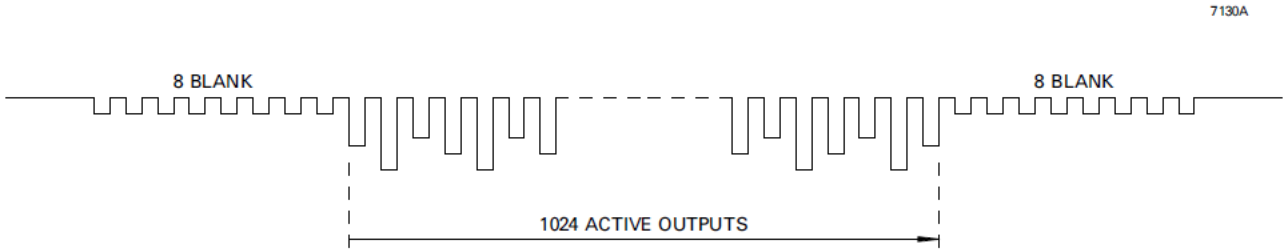
DETAIL OF LINE TRANSFER



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



CLOCK TIMING REQUIREMENTS

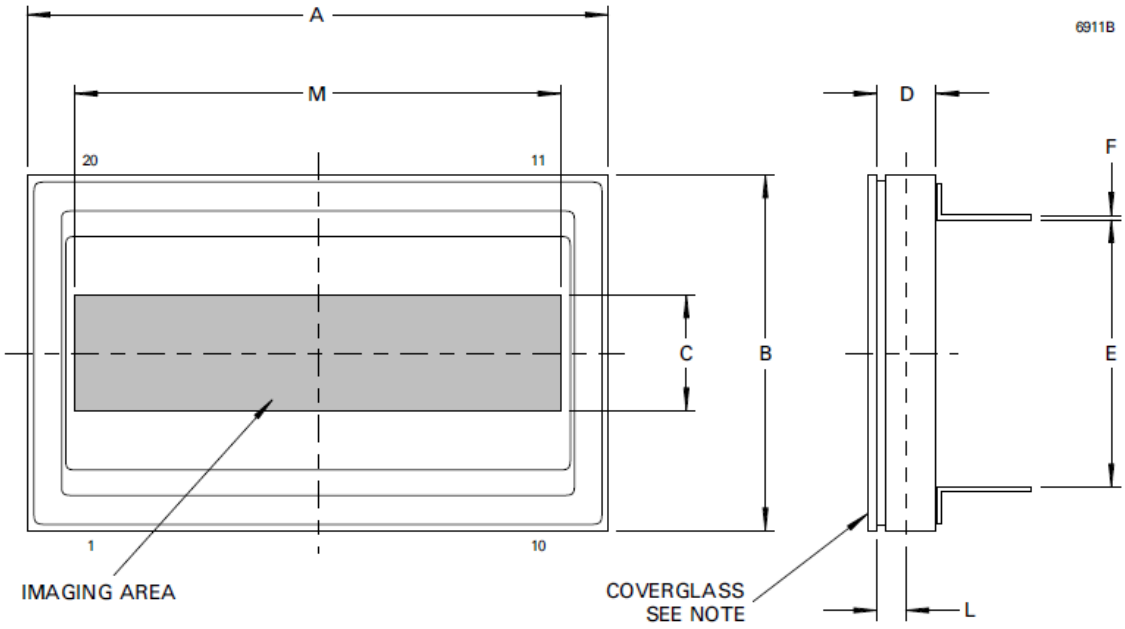
Symbol	Description	Min	Typ	Max	Unit
T_i	Image clock period	50	90	See note 12	µs
t_{wi}	Image clock pulse width	25	45	See note 12	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	5	20	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	20	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	3	10	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	2	10	$0.2T_i$	µs
t_{dir}	Delay time, IØ stop to RØ start	3	10	See note 12	µs
t_{dri}	Delay time, RØ stop to IØ start	1	2	See note 12	µs
T_r	Output register clock cycle period	200	See note 13	See note 12	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.2T_r$	ns
t_{rx} , t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

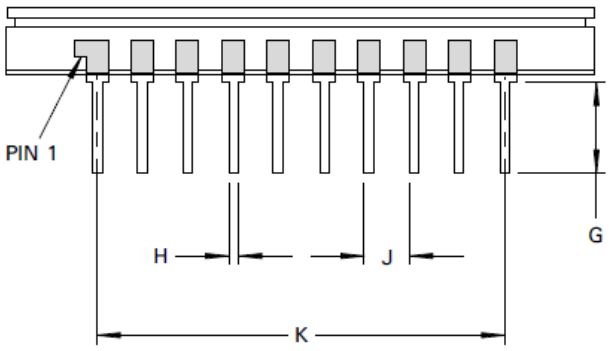
NOTES

12. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
13. As set by the readout period. See note 4.

OUTLINE

(All dimensions without limits are nominal)





Outline Note
The device is normally supplied with a temporary glass window for protection purposes. It can also be supplied with a fixed, quartz or fibre-optic window where required.

Ref	Millimetres
A	32.89 ± 0.38
B	20.07 ± 0.25
C	6.7
D	3.30 ± 0.33
E	15.24 ± 0.25
F	0.254 + 0.051 − 0.025
G	5.21
H	0.46 ± 0.05
J	2.54 ± 0.13
K	22.86 ± 0.13
L	1.65 ± 0.56
M	26.6

ORDERING INFORMATION

Options include:

- Temporary Quartz Window
- Permanent Quartz Window
- Temporary Glass Window

For further information on the performance of these and other options, please contact e2v technologies.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:-

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 3, 4, 6, 7, 8, 9, 12, 19) but not to the other pins.

HIGH ENERGY RADIATION

Device characteristics will change when subject to ionising radiation.
Users planning to operate CCDs in high radiation environments are advised to contact e2v technologies.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	73	–	373	K
Operating	73	233	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface, causing irreversible damage.

Maximum device heating/cooling ..... 5 K/min