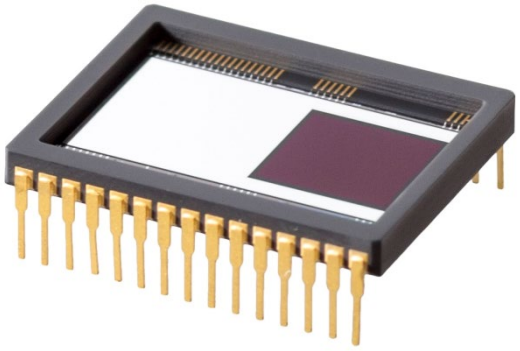
CCD351-00 Back Illuminated, 2-Phase IMO Electron Multiplying CCD Sensor

MAIN FEATURES

- 1024 x 1024 active pixels
- 10µm square pixels
- Variable multiplication gain
- Frame rates of up to 30fps.
- Inverted mode operation for low dark current.
- 30-pin ceramic dual-in-line package



OVERVIEW

The CCD351-00 is a frame transfer, electron multiplying CCD sensor designed for extreme performance in high frame rate ultra-low light applications. The Teledyne e2v back-thinning process ensures high quantum efficiency over a wide range of wavelengths.

The device functions by converting photons to charge in the image area during the integration time period, then transferring this charge through the image and store sections into the readout register. Following transfer through the readout register, the charge is multiplied in the gain register prior to conversion to a voltage by a low noise output amplifier.

The multiplication gain in the readout chain allows L3Vision™ devices to effectively eliminate readout noise. The gain may be varied from 1× to over 1000× by adjustment of the multiplication phase amplitude RØ2HV.

GENERAL DATA

Image section	1024 x 1024
Pixel size	10 µm × 10 µm
Active image area	10.24 × 10.24 mm
Package size	22.86 × 28.00 mm
Amplifier responsivity	3.0 µV/e^-
Readout noise with CDS	<<1e^- with EM gain 50e^- at unity gain
Output data rate	37 MHz
Active pixel charge storage	35 ke^-/pixel
Dark signal (18°C)	100 e^-/pixel/s

ORDERING INFORMATION

CCD351-00-G-XYZ
G = cosmetic grade
XYZ= specific variant type (e.g. AR coating)
e.g. XYZ = G47 for basic process with midband coating

Teledyne UK Limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom Teledyne UK Ltd. is a Teledyne Technologies company.
Telephone: +44 (0)1245 493493 Facsimile: +44 (0)1245 492492
Contact Teledyne e2v by e-mail: Enquiries@Teledyne-e2v.com or visit www.teledyne-e2v.com for global sales and operations centres.

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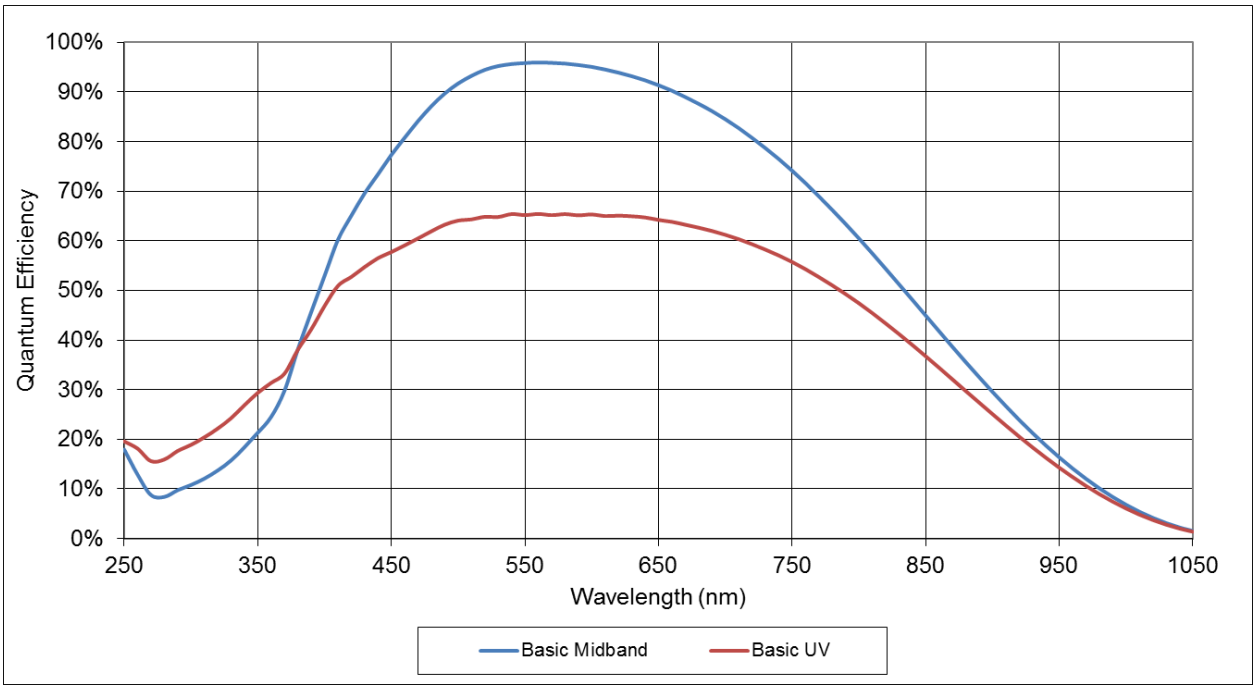
IMAGING PERFORMANCE

ELECTRO-OPTICAL PERFORMANCE

	Minimum	Typical	Maximum	Units	Notes
Peak charge storage (image)	25	35	-	ke$^-$/pixel	Note 1
Peak charge storage (register)	100	145	-	ke$^-$/pixel	Note 1
Output amplifier responsivity	2.7	3.0	3.4	µV/e$^-$	Note 1
Readout noise with CDS	-	<<1 with EM gain 50 at unity gain	-	e$^-$ rms	Note 2
Read-out frequency	-	37	-	MHz	Note 3
Dark signal at 18°C	-	100	250	e$^-$/pixel/s	Note 1
Charge transfer efficiency: parallel serial		 99.999 99.999	 - -	 % %	Note 4

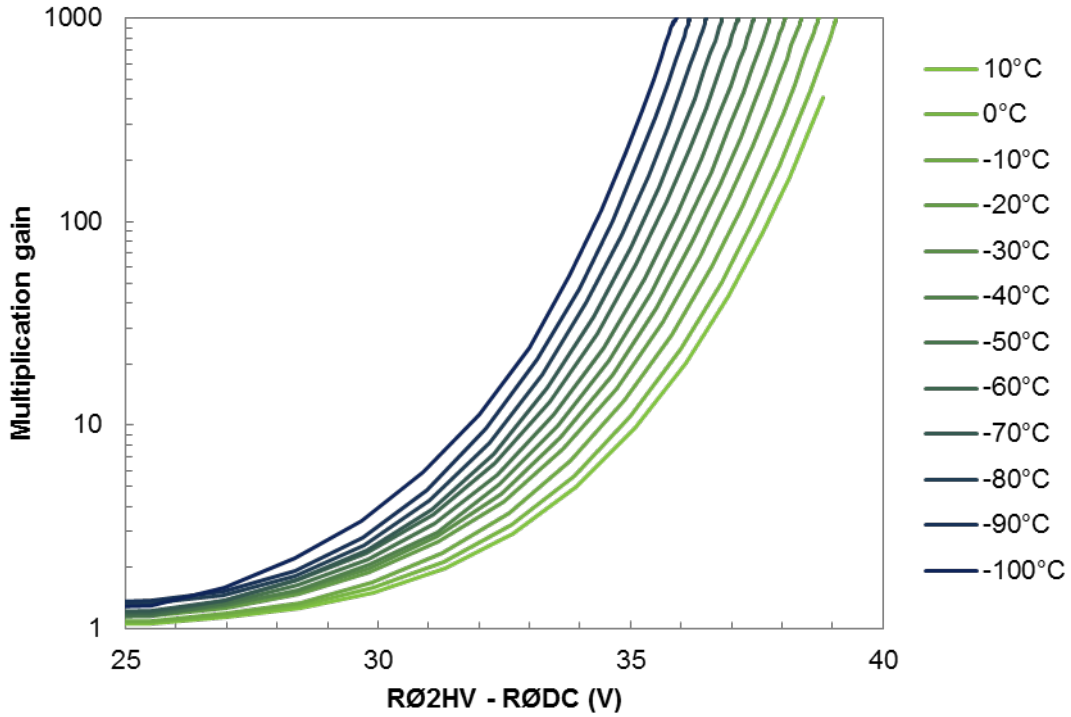
Notes
Note 1. Measured at 18°C with typical operating voltages.
Note 2. Inferred by design, not measured.
Note 3. Depending on the external load capacitance to be driven.
Note 4. At unity gain.

TYPICAL SPECTRAL RESPONSE (At -20°C, no window, 10µm thickness) (not measured)

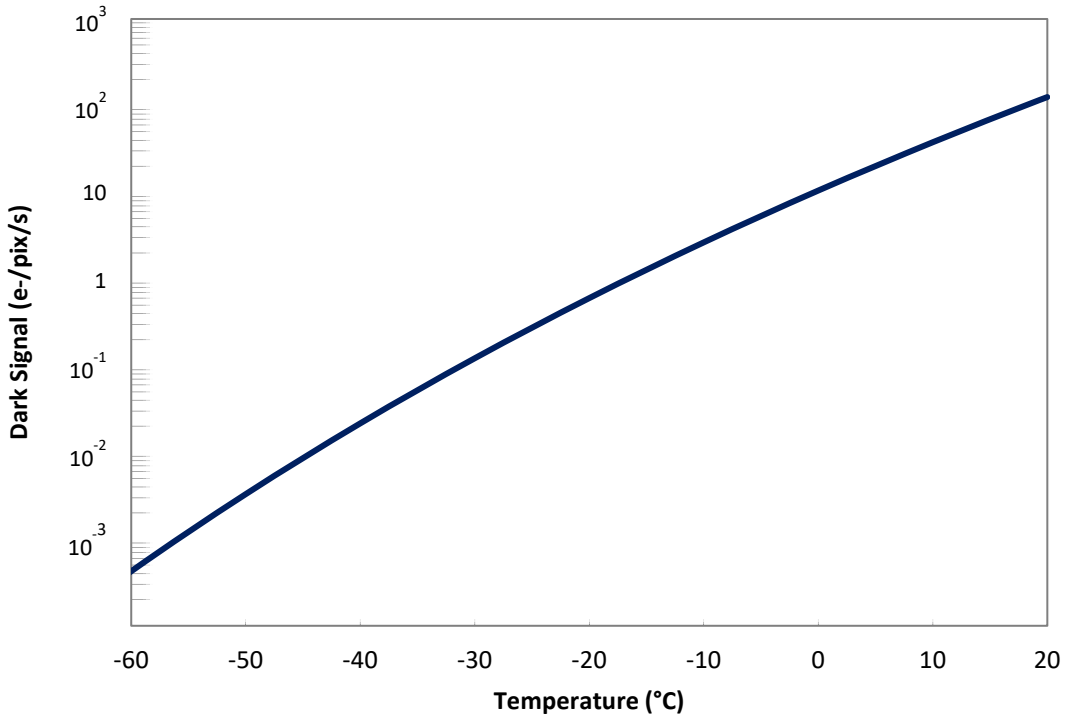


Devices can be supplied with alternative anti-reflection coatings optimised for different wavelengths – details from Teledyne e2v.

VARIATION OF MULTIPLICATIVE GAIN WITH RØ2HV MINUS RØDC



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE



DEFECT DEFINITIONS

All cosmetic tests are performed at 18 ± 3ºC in 2-phase inverted mode at 30fps with x1000 multiplicative gain.

SPECIFICATION

Parameter	Grade 1
White Defects	24
White Columns	0
Black/Pin-head Columns	1

Grade 5 devices are functional but with an image quality below grade 1. Other specifications may also not be met or may not have been tested.

Note: incorrect biasing of the device may result in spurious dark or white blemishes appearing. These will be eliminated if the biases are adjusted.

WHITE COLUMNS

White defects are pixels having a dark signal generation rate corresponding to an output signal of greater than 5 times the maximum dark signal level. A white column contains at least 9 white defects.

BLACK COLUMNS

Black defects are counted when they have a responsivity of less than 80% of the local mean signal at approximately the specified gain and level of illumination. A black column contains at least 9 black defects.

PIN-HEAD COLUMNS

Pin-head columns are manifest as a partial dark column with a bright pixel showing photo-response at the end of the column nearest to the readout register. Pin-head columns are counted when the black column has a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A pin-head column contains at least 9 black defects.

DEVICE DESCRIPTION

FIGURE 1: DEVICE ARCHITECTURE

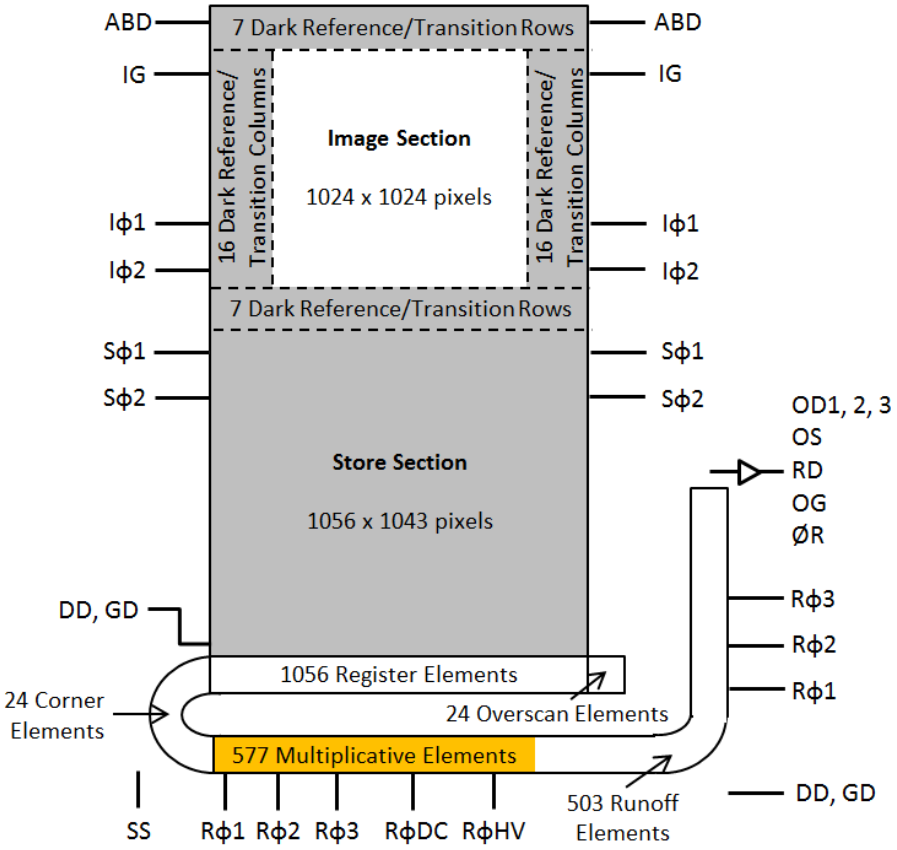
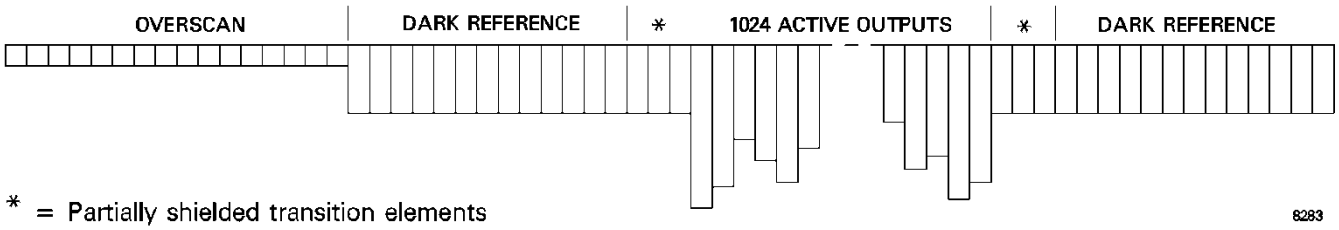


FIGURE 2: LINE OUTPUT FORMAT



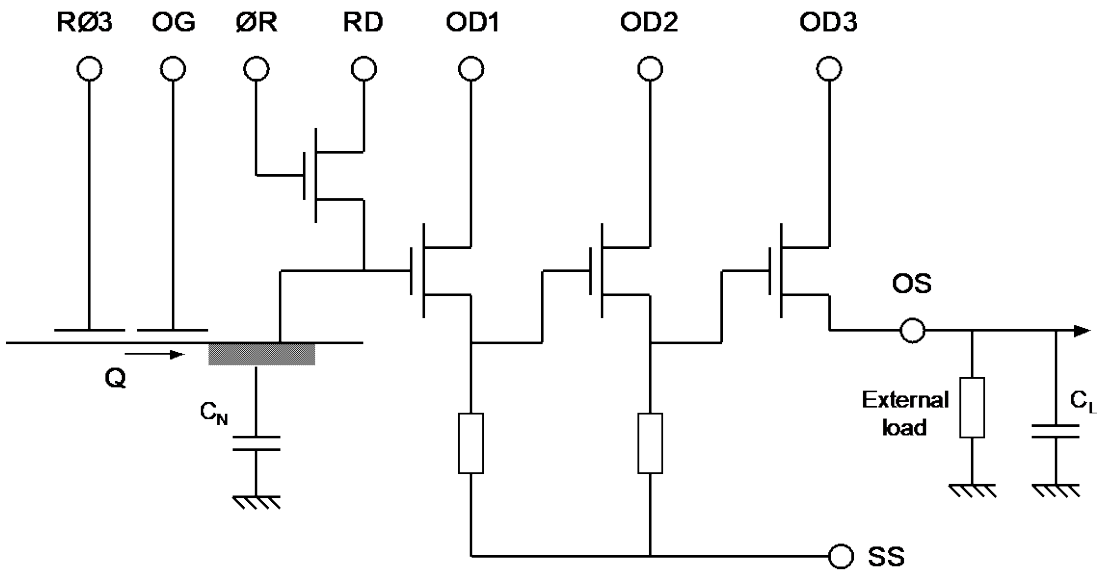
ONE ROW PIPELINE READOUT DELAY MODE

- In this mode, there are 1080 clock cycles per row, consisting of 24 overscan, 13 dark reference, 3 transition, 1024 active, 3 transition and 13 dark reference elements.
- There will be a one row propagation delay between transferring a row from the store section to the conventional register and then reading it out through the CCD output.

FULL REGISTER READOUT MODE

- In some situations, it be may be preferable to clock ≥ 2160 clock cycles per row to read out all the elements from the beginning of the conventional register through to the CCD output.
- In this case, the number of overscan elements is increased by 1080.

FIGURE 3: OUTPUT CIRCUIT



- The external load is a 2kΩ resistor or a 6mA constant-current type.
- Note that 1.5mA quiescent current flows through SS.
- The output impedance is typically 90Ω.

ELECTRICAL PERFORMANCE

PIN DESCRIPTIONS

The table below gives the pin connections and functions

Pin	Ref	Function		Ref	Function	Pin
1	SS	Substrate		SS	Substrate	**30**
2	ABD	Anti-blooming drain [Note 5]		IØ1	Image section clock phase 1	**29**
3	IG	Isolation gate		IØ2	Image section clock phase 2	**28**
4	SS	Substrate		SØ1	Store section clock phase 1	**27**
5	SS	Substrate		SØ2	Store section clock phase 2	**26**
6	OD1	Output drain 1		RØ1	Register clock phase 1	**25**
7	OD2	Output drain 2		RØ2	Register clock phase 2	**24**
8	SS	Substrate		RØ3	Register clock phase 3	**23**
9	OD3	Output drain 3		SS	Substrate	**22**
10	OS	Output source		n.c.	No connection [Note 6]	**21**
11	RD	Reset drain		SS	Substrate	**20**
12	OG	Output gate		ØR	Output reset pulse	**19**
13	DD	Dump drain		RØ2HV	Register clock phase 2 HV	**18**
14	n.c.	No connection		RØDC	Register DC phase	**17**
15	SS	Substrate		SS	Substrate	**16**

Notes
Note 5. Can be tied to DD or RD for non-antibloomed devices.
Note 6. Front-face output source connection.

OPERATING VOLTAGES

Typical operating voltages are as given in the table below. Some adjustment within the minimum-maximum range specified may be required to optimise performance.

Clock	Description	Clock or DC Level (V)			Max rating with respect to SS	Notes
		Min	Typical	Max		
VSS	Substrate voltage	3	4	5	-	Note 7
VDD	Dump drain voltage	IØ high + 1	20	-	-0.3 and +25	
IØ high	Image section: clock high	IØ low + 7	5	10	±20	
IØ low	Image section: clock low	-	-5	-	-	Note 8
SØ high	Store section: clock high	SØ low + 7	5	10	±20	
SØ low	Store section: clock low	-	-5	-	-	
RØ high	Register: clock high	RØ low + 6	10		±20	
RØ low	Register: clock low	-3	0		-	Note 9
R2HVØ high	Register HV phase high	38	42	43	-20 and +50	Note 10
RØHV low	Register HV phase low	-	0	-	-	Note 9
RØDC	Register DC phase	RØ low + 3.5	4.5	6.0	±20	Note 11
VOG	Output gate voltage	1	2	3	±20	
VIG	Isolation gate voltage		-5		±20	
VABD	Anti-blooming drain voltage	VIG high + 12.5	20	22	-0.3 and +25	
ØR high	Reset clock high	8	10	12	±20	
ØR low	Reset clock low	0	0	1	-	
VRD	Reset drain voltage	13	15	VOD1 - 0.5	-0.3 and +25	Note 12
VOD1	Output drain 1 voltage	VRD + 0.5	15.5	16	-0.3 and +32	Note 12
VOD2	Output drain 2 voltage	11	13	VOD1	-0.3 and +32	Note 12
VOD3	Output drain 3 voltage	9	11	VOD2	-0.3 and +32	Note 12
VOS	Output source					Note 13

Notes

Note 7. Reference level for all maximum ratings.
Note 8. For inverted mode operation.
Note 9. Register clock low should not be taken near pinning or significant serial clock induced charge will result when operated with multiplication gain.
Note 10. Typical RØ2HV for specified gain of 500 at 18°C.
Note 11. Should be optimised for correct serial charge transfer and performance at high gain.
Note 12. Output biases set at zero glow conditions. At voltages exceeding 2V above these settings amplifier glow is considerable.
Note 13. See details of output circuit. The current through the pin must not exceed 20 mA. Permanent damage may result if, in operation, OS experiences short circuit conditions.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode Capacitances at Mid Clock Levels (Calculated From Design)			
Connection	Capacitance to SS	Total Inter-phase Capacitance	Units
IØ1	3.4	3.7	nF
IØ2	3.4	3.7	nF
SØ1	6.5	3.7	nF
SØ2	4.7	3.7	nF
RØ1	50	56	pF
RØ2	40	37	pF
RØ3	50	49	pF
RØ2HV	30	19	pF

TIMING

CLOCK TIMING REQUIREMENTS

Drive pulse waveform specification – for typical voltages.

Symbol	Description	Minimum	Typical	Units	Notes
T_{ft}	Frame Transfer Period	1200	1350	ns	
T_{lt}	Line Transfer period	1520	1730	ns	
t_{wh}	Image & Store clock high duration	900	1000	ns	
t_{wl}	Image & Store clock low duration	300	350	ns	Note 14
t_o	Image & Store clock overlap	300	350	ns	Note 14
t_{whi}	Initial IØ1 high.	1.0	1.5	µs	Note 15
t_{drt}	Delay time, RØ stop to SØ start	20	30	ns	
t_{dtr}	Delay time, SØ stop to RØ start	300	350	ns	Note 16
-	Image & Store pulse rise & fall time (10 to 90%)	100	150	ns	
-	RØ1, RØ2 & RØ3 pulse rise & fall time (10 to 90%)	4	8	ns	
-	RØ2HV pulse rise and fall time (10 to 90%)	6	12	ns	Note 17
-	Reset pulse rise and fall times (10 to 90%)	2	3	ns	
-	RØ1, RØ2 & RØ3 pulse overlap	-	70	% of amplitude	
-	Reset pulse width	5	10	ns	
-	Delay time, ØR low to RØ3 high	0	1	ns	

Notes

Note 14. Typical timing for clocking of near full well at typical voltages. Lower signal levels may be able to be clocked faster without loss of charge transfer efficiency.
Note 15. The optimum time period for this parameter may depend on the scene signal level.
Note 16. Ensure adequate settling time after store clock cycle before initiating register readout.
Note 17. A sine wave can also be used.

FIGURE 4: FRAME TRANSFER CLOCKING

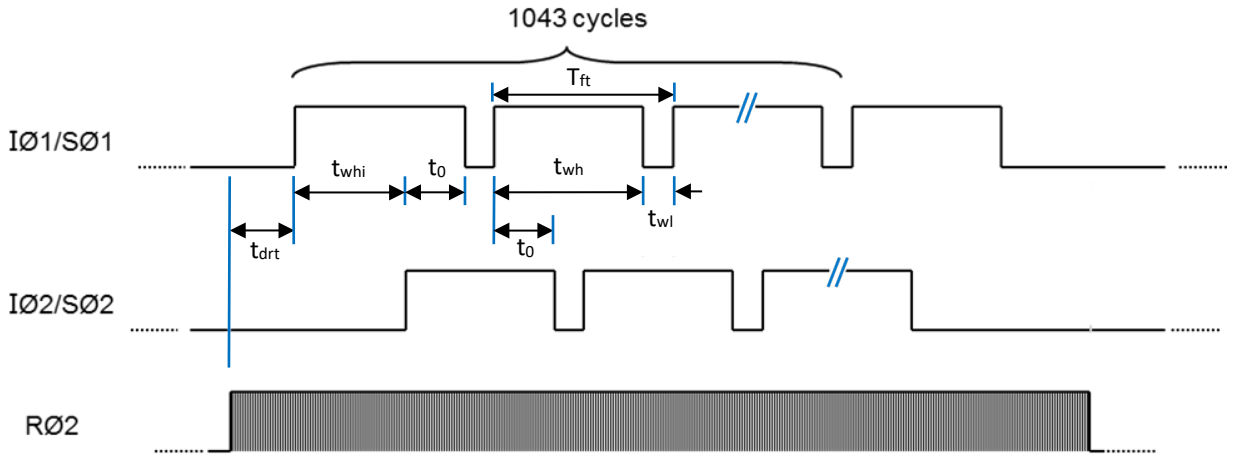


FIGURE 5: DETAIL OF LINE TRANSFER

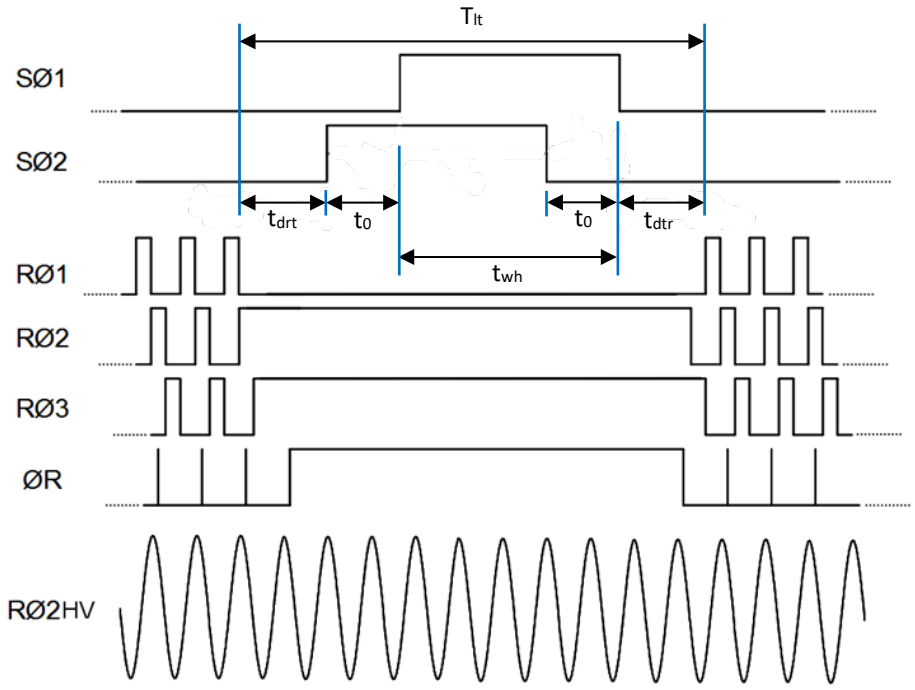
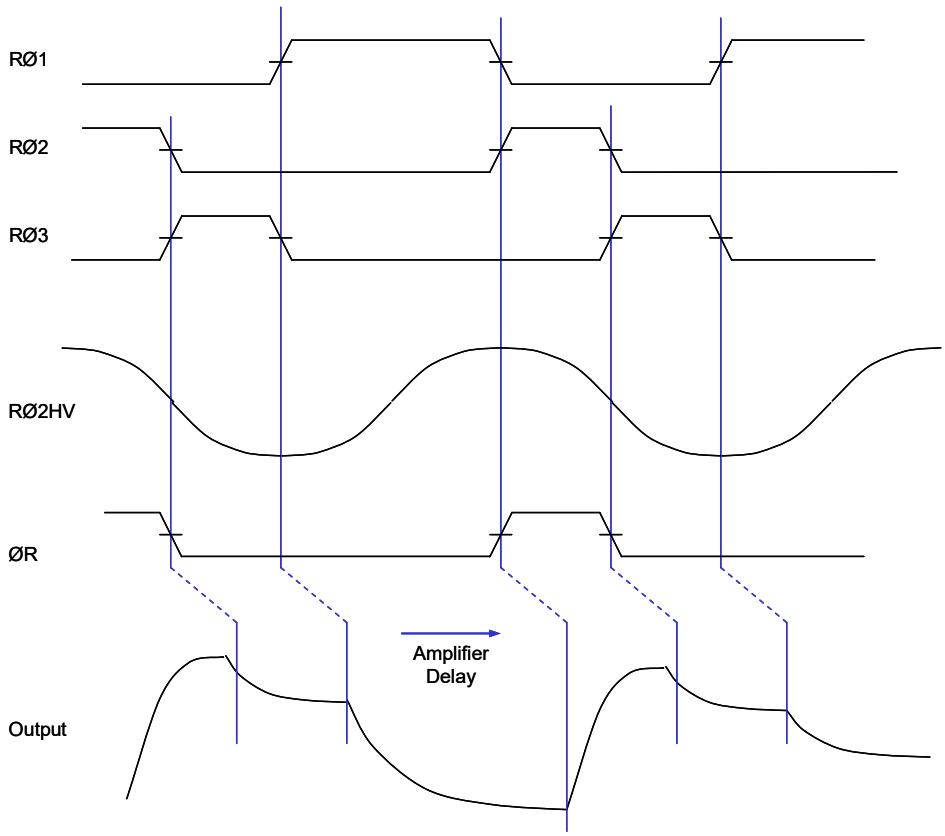
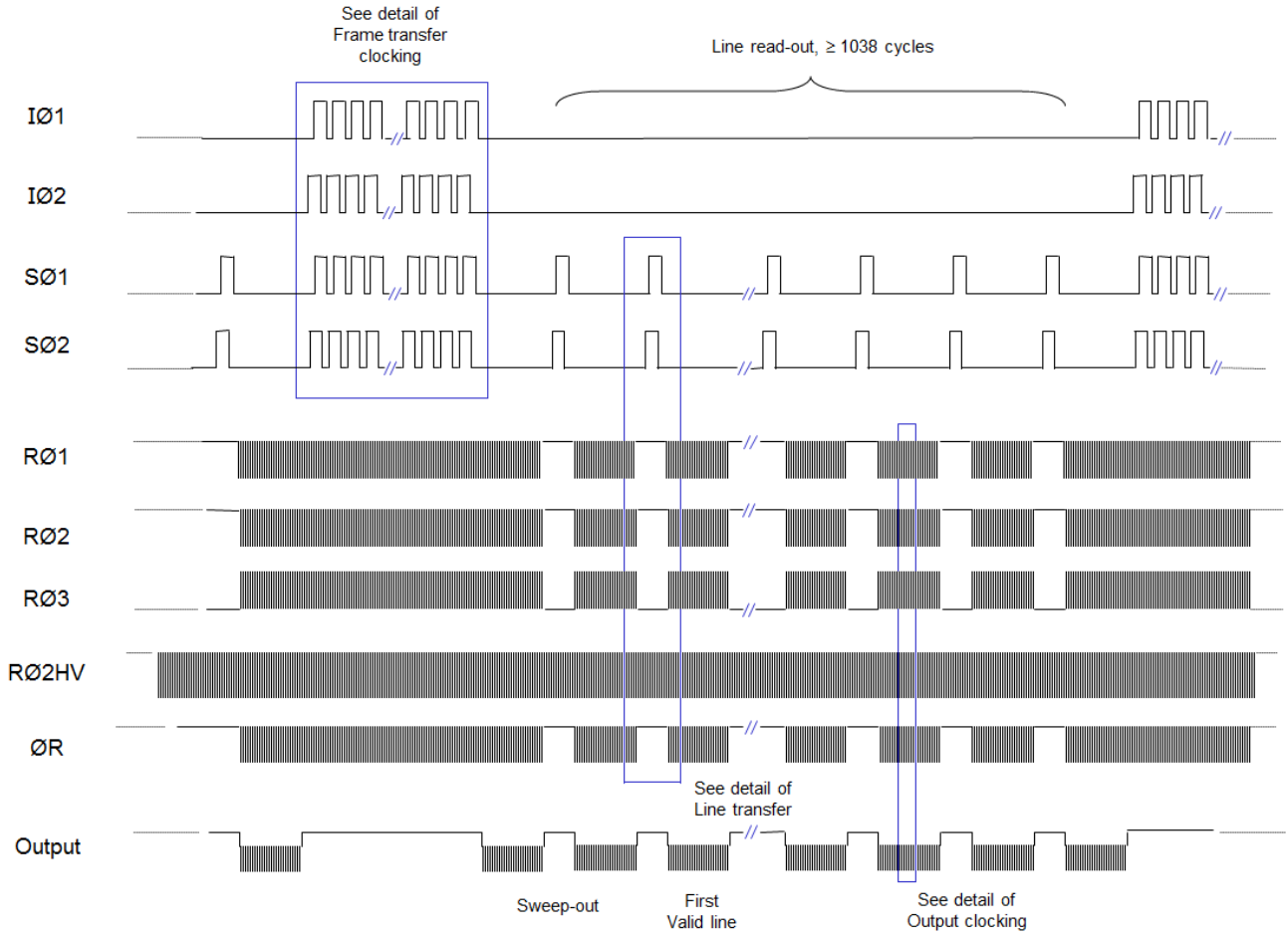


FIGURE 6: DETAIL OF OUTPUT CLOCKING



Note: the time delay introduced by the amplifier, as indicated, is likely to be significant in relation to the total pixel period.

FIGURE 7: FRAME READOUT TIMING DIAGRAM



POWER CONSUMPTION

The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from the parallel and serial clocking (i.e. driving the capacitive loads).

The table below gives theoretical values for the components of the on-chip power dissipation calculated from the design for the case of a device running at 30 fps with a readout frequency of 37 MHz and a sinusoidal RØ2HV waveform at 40V.

Component	Power Dissipation (mW)
Amplifier	65
Serial clocks	435
Parallel clocks	85
Total	**585**

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Furthermore, unlike most Teledyne e2v devices, the CCD351 is NOT provided with anti-static protection devices on all gate connections – during operation RØ2HV requires a high voltage peak amplitude for gain multiplication that is not compatible with standard gate protection structures. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench.
- Operator wearing a grounded wrist strap.
- All receiving sockets to be positively grounded.

Evidence of incorrect handling will invalidate the warranty.

The devices are assembled in a clean room environment and Teledyne e2v recommend that similar precautions are taken by the user to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to ionising radiation. Characterisation data is held at Teledyne e2v with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

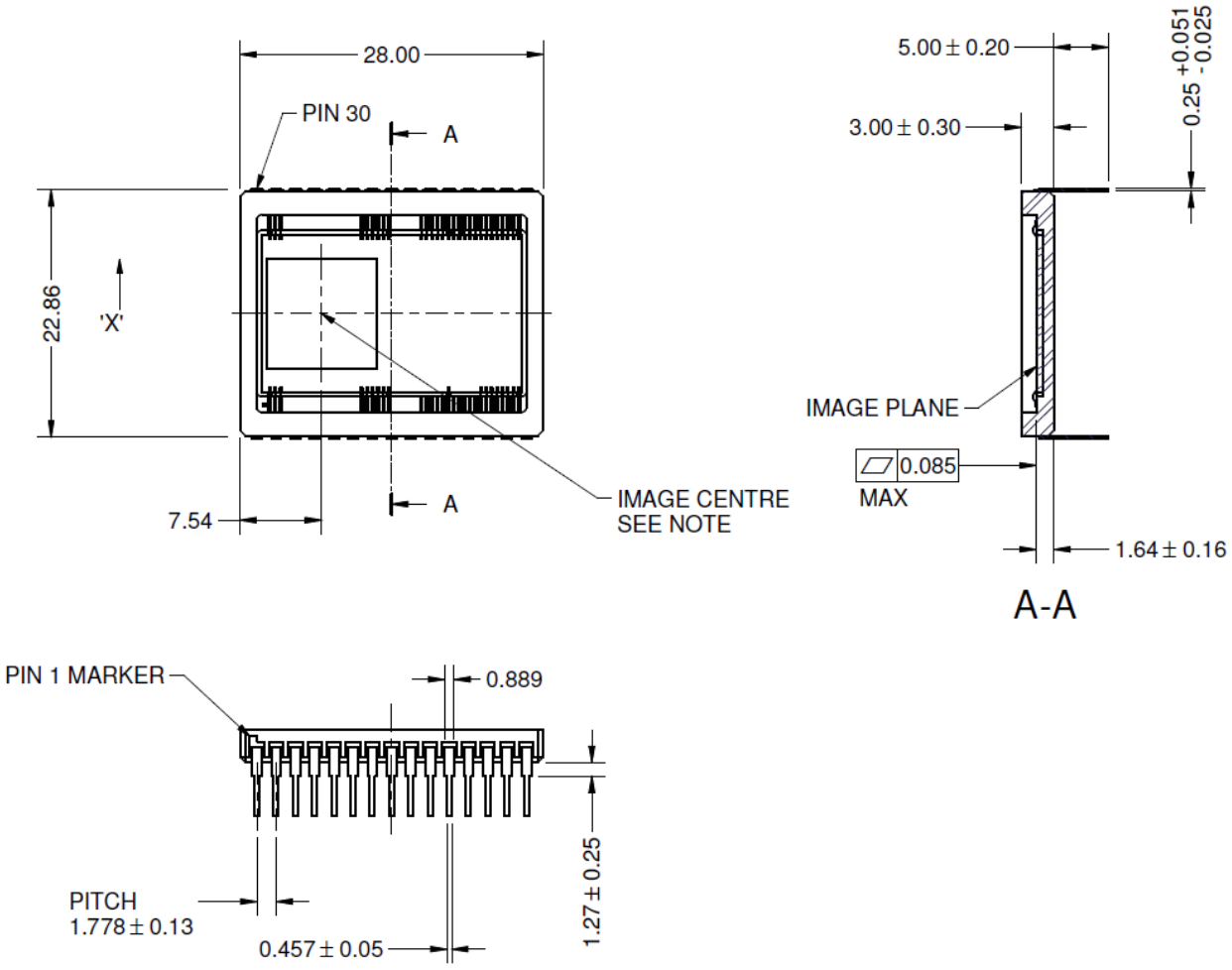
STORAGE AND OPERATING TEMPERATURES

Component	Min	Max
Operating Temperature	-120°C	+75°C
Storage Temperature	-200°C	+100°C
Rate of change		±5°C/min

Note: Operation or storage in humid conditions may give rise to ice on the surface when the sensor taken to low ambient temperatures, thereby causing irreversible damage. Full performance is only guaranteed at the nominal operating temperature of 18°C.

GEOMETRY

FIGURE 8: PACKAGE OUTLINE



Note: The image centre is aligned centrally in the package in direction ‘X’, to within a tolerance of ±0.20mm.