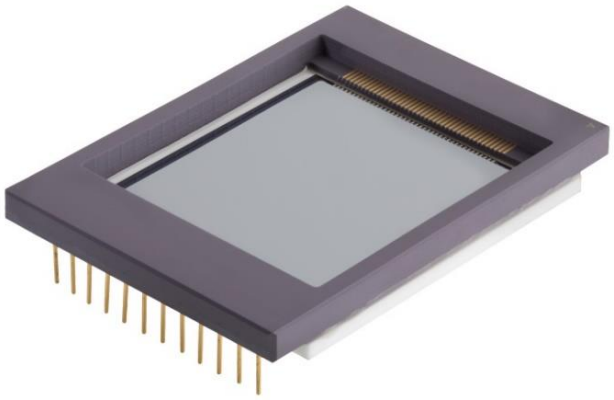
CCD42-40

4MP BSI CCD Sensor



KEY FEATURES

- Back Illuminated for high quantum efficiency
- Full-frame operation
- Symmetrical anti-static gate protection
- Very low noise output amplifiers
- Dual responsivity output amplifiers
- Gated Dump drain on output register
- Compact footprint package
- Deep depletion options for Red/NIR
- Uncoated options for soft X-Ray

TYPICAL APPLICATIONS

- Scientific Imaging
- Microscopy
- Medical Imaging
- Astronomy

PART REFERENCES

Please see last page for full list of available parts.

GENERAL DATA

Format	
Image Area	27.6 x 27.6 mm
Active Pixels	2048 (H) x 2048 +4 (V)
Pixel Size	13.5 x 13.5 µm
Number of output amplifiers	2
Number of underscan (serial) pixels	50
Package	
Package Size	37.0 x 51.7 mm
Number of Pins	24
Inter-pin Spacing	2.54 mm
Inter-row Spacing	45.72 mm
Window Material	Removable Glass
Package type	Ceramic DIL array
Performance	
Maximum readout frequency	3 MHz
Output amplifier sensitivity	4.5 µV/e^-
Peak signal (NIMO)	150 ke^-/pixel
Peak signal (AIMO)	100 ke^-/pixel
Dynamic range (NIMO)	50,000:1
Dynamic range (AIMO)	33,333:1
Spectral range	200 – 1060 nm
Readout noise	3 e^- rms
Peak output voltage	675 mV

OVERVIEW

Back illumination technology, in combination with extremely low noise amplifiers, makes the device well suited to demanding scientific applications requiring a high dynamic range.

There are two low noise amplifiers in the read out register, one at each end. Charge can be made to transfer through either or both amplifiers by making the appropriate R∅ connections. The readout register has a gate controlled dump drain to allow fast dumping of unwanted data.

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1B300000-A1A Version 1, January 2024
Template: 1B300000-DFP Ver 1
CM 5003491

Approved for public release: Teledyne e2v APPROVED

PERFORMANCE

NIMO

Parameter		Min	Typical	Max	Units	Note
Peak charge storage		80,000	150,000		e^-/pixel	1
Peak output voltage (unbinned)			675		mV	3
Dynamic range			50,000:1			4
Dark signal at 293 K	Standard Silicon		20,000	45,000	e^-/pixel/s	2, 9
Dark signal at 153 K	Deep Depleted Silicon		0.2	1	e^-/pixel/hr	2, 8
Charge transfer efficiency	Parallel	99.999	99.9999	-	%	5
	Serial	99.999	99.9993	-		
Output amplifier responsivity	Low noise mode	3	4.5	6	µV/e^-	3
	High signal mode		1.5			
Readout noise	Low noise mode		3	4	rms e^-/pixel	6
	High signal mode		6			3
Readout frequency			45	3000	kHz	7
Output node capacity			1,000,000		e^-	3, 11
Output Non-Linearity		-1.5	-	+1.5	%	12

AIMO

Parameter		Min	Typical	Max	Units	Note
Peak charge storage		80,000	100,000		e^-/pixel	1
Peak output voltage (unbinned)			450		mV	
Dark signal at 293 K			250	500	e^-/pixel/s	2, 3
Dynamic Range			33,333:1			4
Charge transfer efficiency	Parallel	99.999	99.9999	-	%	5
	Serial	99.999	99.9993	-		
Output amplifier responsivity	Low noise mode	3	4.5	6	µV/e^-	3
	High signal mode		1.5			
Readout noise at 253 K	Low noise mode		3	4.5	rms e^-/pixel	3,6
	High signal mode		6			
Readout frequency			20	3000	kHz	7
Dark Signal non-uniformity at 293 K (std. deviation)			60	125	e^-/pixel/s	3, 10
Output node capacity			1,000,000		e^-	11

NOTES

1. Signal level at which resolution begins to degrade. The typical values are those expected from design.
2. The typical average (background) dark signal at any temperature T (kelvin) between 230 K and 300 K may be estimated from:

NIMO: $Q_d/Q_{d0} = 122T^3e^{-6400/T}$

AIMO: $Q_d/Q_{d0} = 1.14 \times 10^6T^3e^{-9080/T}$

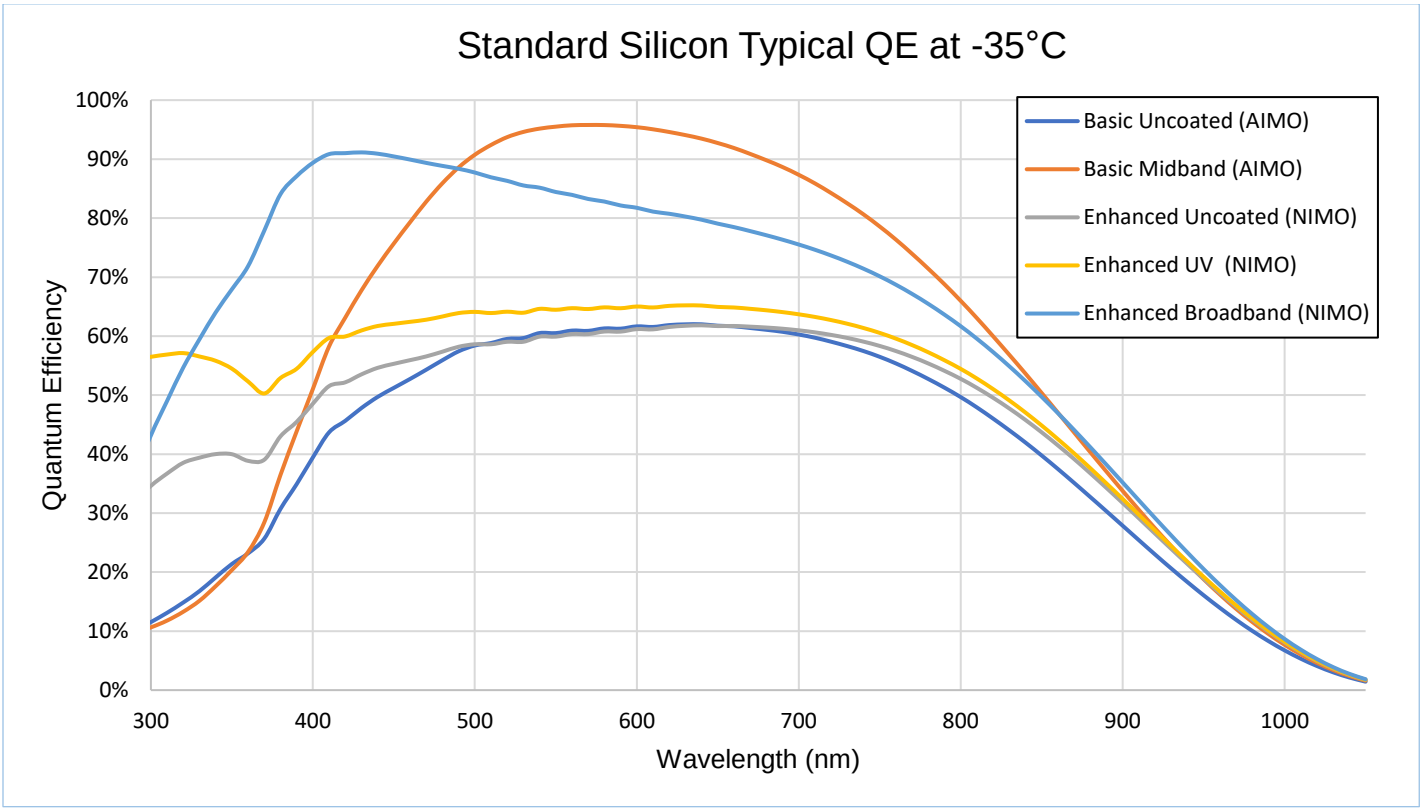
where Q_{d0} is the dark signal at 293 K.

3. Test carried out at Teledyne e2v on all sensors.
4. Dynamic range is the ratio of full-well capacity to readout noise measured at 253 K and NIMO readout frequency of 18 kHz and AIMO at 20 kHz.
5. CCD characterisation measurements made using charge generated by X-rays of known energy.
6. Measured using dual slope integrator technique (i.e. Correlated double sampling). NIMO measured at read out frequency of 18 kHz and AIMO at 20 kHz.
7. Readout above 3 MHz can be achieved but performance to the parameters given cannot be guaranteed.
8. Measured at 188 K, excluding white defects with substrate at 3 V
9. Measured at 238 K, excluding white defect with substrate held high.
10. Measured between 253 K and 293 K, excluding white defects.
11. With output circuit configured in low responsivity/high-capacity mode (OG2 high).
12. Non-linearity measured over the signal range 20-150 ke^- with pixel binning.

SPECTRAL RESPONSE

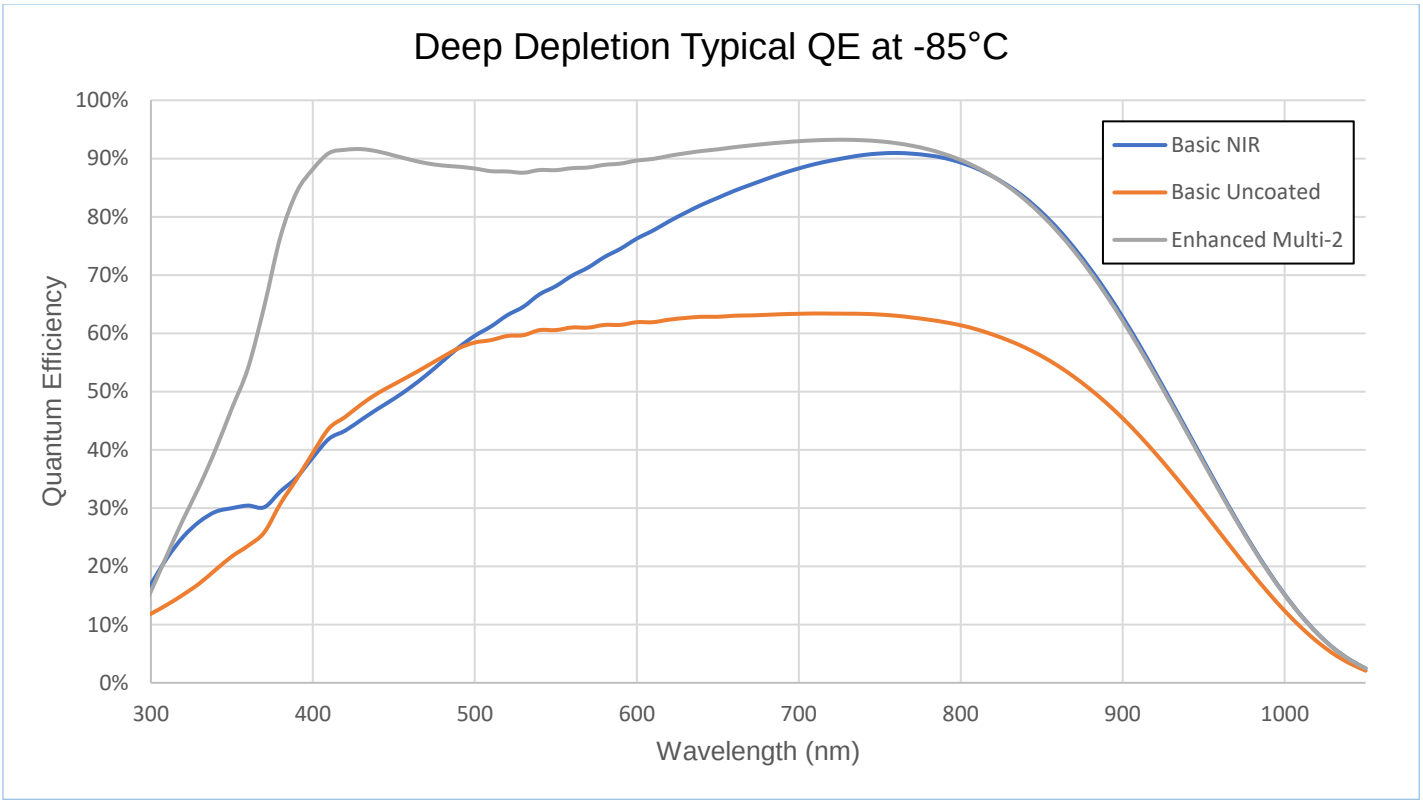
Standard Silicon at 238K (-35°C)

Wavelength (nm)	Minimum Response (QE)				Maximum Response Non-uniformity (1σ)	
	Enhanced Process UV Coated	Enhanced Process Broadband Coated	Basic Process Midband Coated	Basic Process Uncoated		
300	45	-	-	-	-	**%**
350	45	50	15	10	-	**%**
400	55	80	40	25	3	**%**
500	60	80	85	55	-	**%**
650	60	75	85	50	3	**%**
900	30	30	20	20	5	**%**



Deep Depleted Silicon at 188 K (-85°C)

Wavelength (nm)	Minimum Response (QE)			Maximum Response Non-uniformity (1σ)	
	Basic Process NIR (ER1 900 nm) Coated	Enhanced Process Multilayer 2 Coated	Basic Process Uncoated		
300	-	-	-	-	%
350	-	30	10	-	%
400	25	75	25	3	%
500	45	75	50	-	%
650	75	80	55	3	%
900	45	50	40	5	%



COSMETIC SPECIFICATION

Standard Silicon

Grade	0	1
Column defects; black or white	0	3
Black spots	100	150
White spots	100	150
Traps >200 e^-	10	20

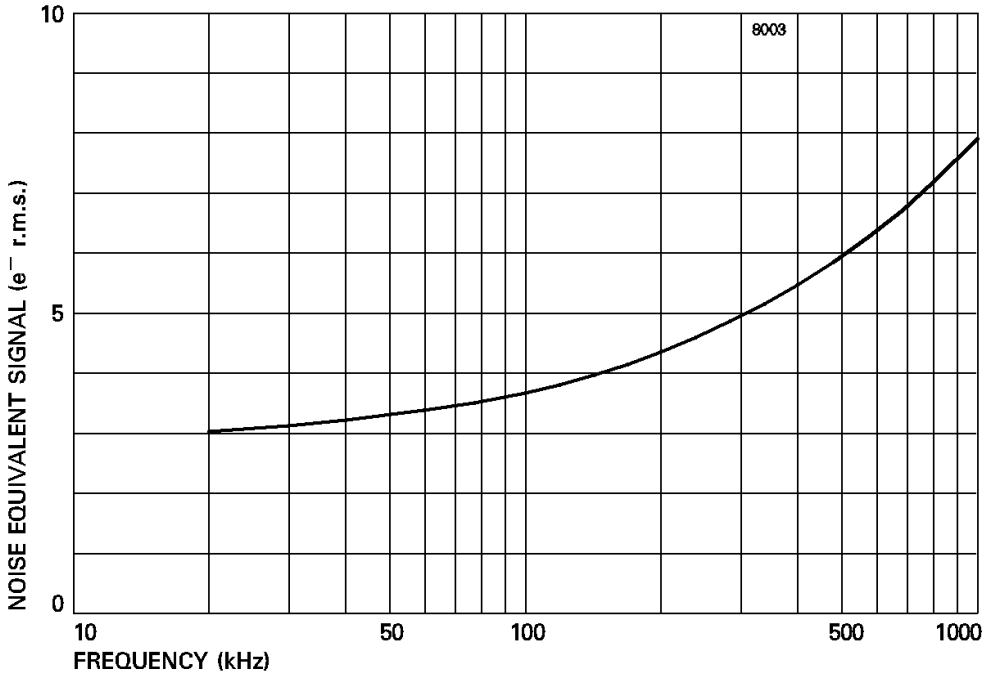
Deep Depleted Silicon

Grade	0	1
Column defects; black or white	3	6
Black spots	250	500
White spots	250	500
Traps >200 e^-	20	30

Cosmetic definitions

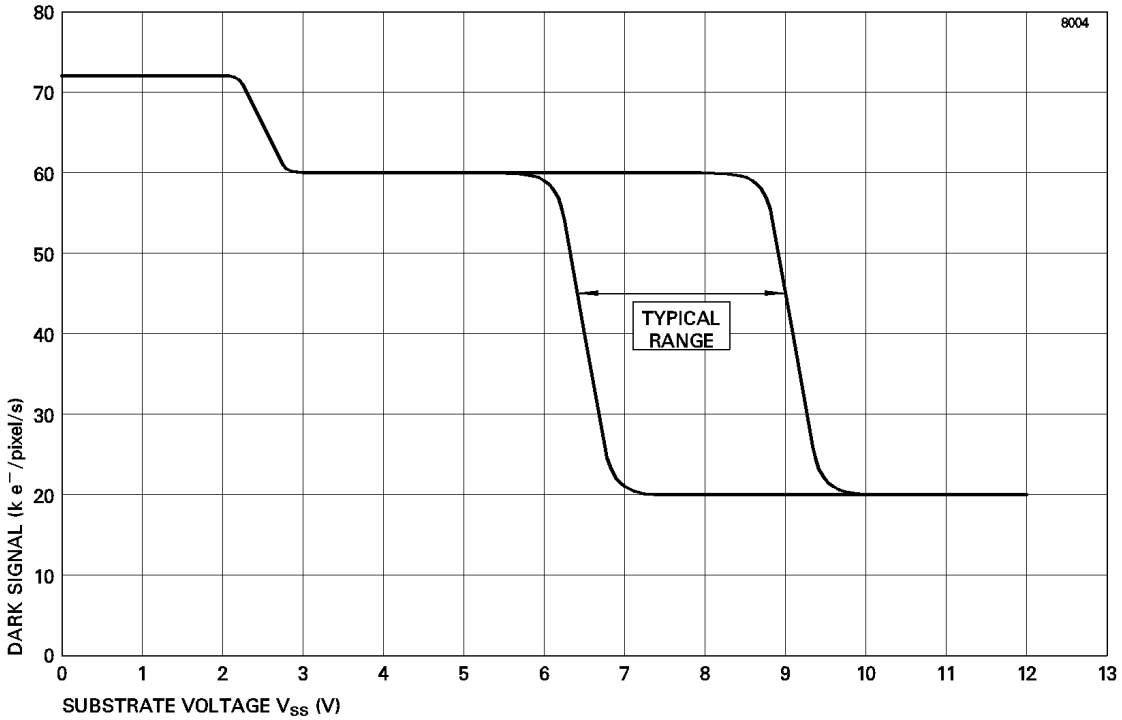
Traps	Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^-. Traps will be observed less at higher temperatures, but more may appear below 243K.
Black Spots	Are counted when they have a signal level of less than 80% of the local mean at a signal level of approximately half full-well.
White Spots (NIMO)	Are counted when they have a generation rate 20 times the specified maximum dark signal generation rate (measured between 243 and 293 K). The amplitude of white spot blemishes decreases rapidly with temperature and is given by: $Q_d/Q_{d0} = 122T^3e^{-6400/T}$
White Spots (AIMO)	Are counted when they have a generation rate 125 times the specified maximum dark signal generation rate (measured between 253 and 293 K). The amplitude of white spot blemishes decreases rapidly with temperature and is given by: $Q_d/Q_{d0} = 122T^3e^{-6400/T}$
Column Defects	A column which contains at least 50 white or 50 black defects.

TYPICAL OUTPUT CIRCUIT NOISE (if measured using clamp and sample)

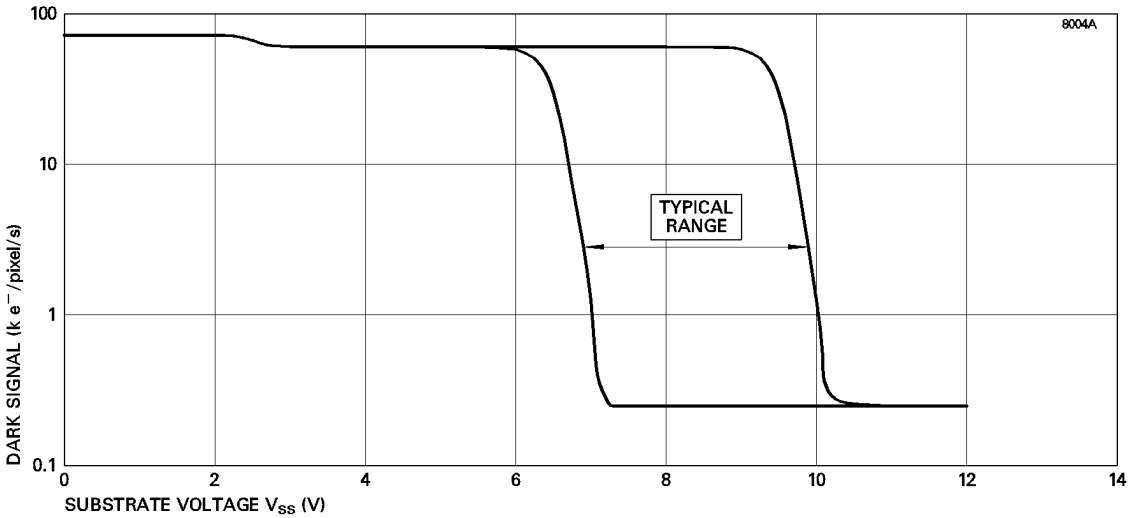


TYPICAL VARIATION OF DARK CURRENT WITH SUBRATE VOLTAGE AT 20°C

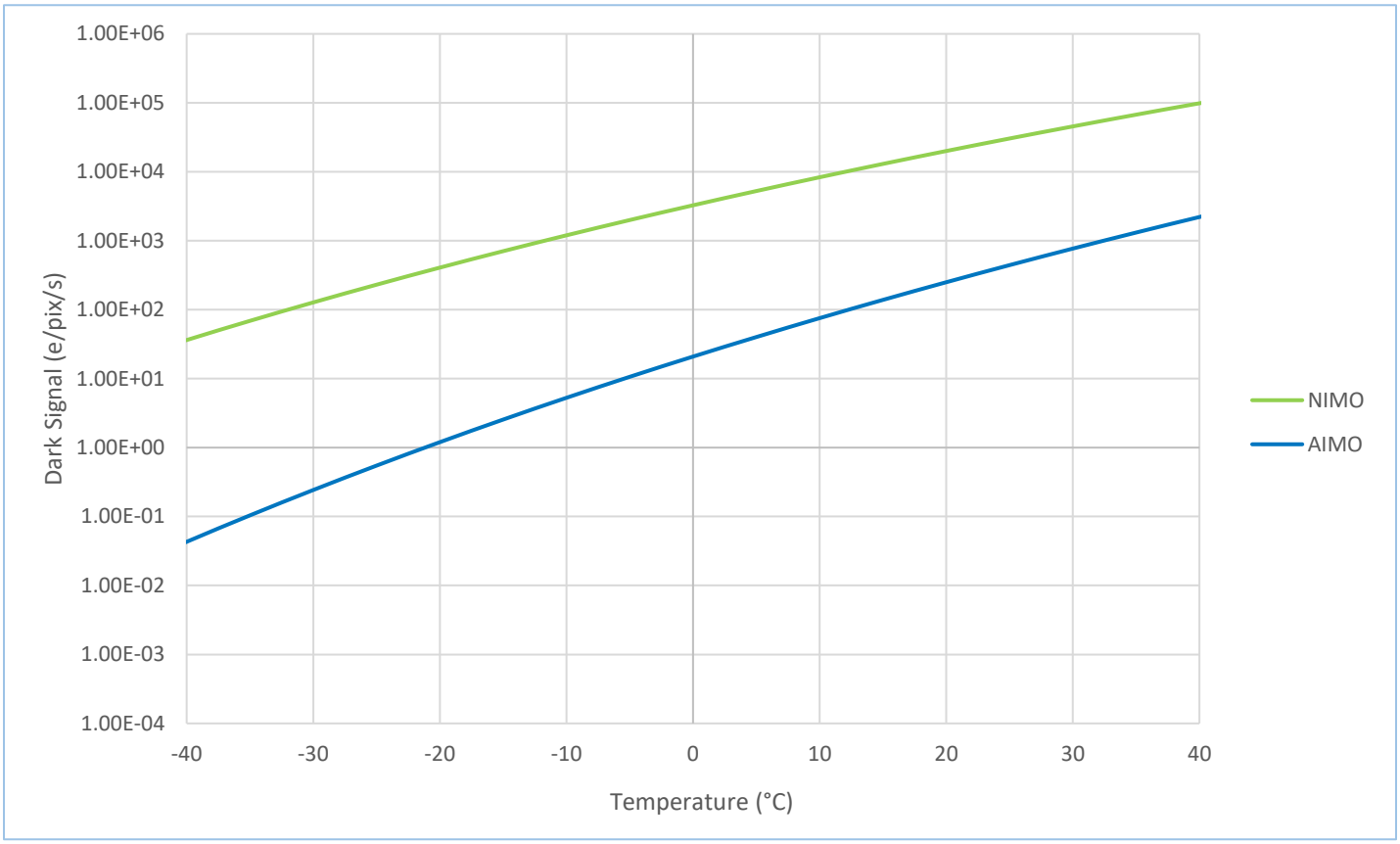
NIMO



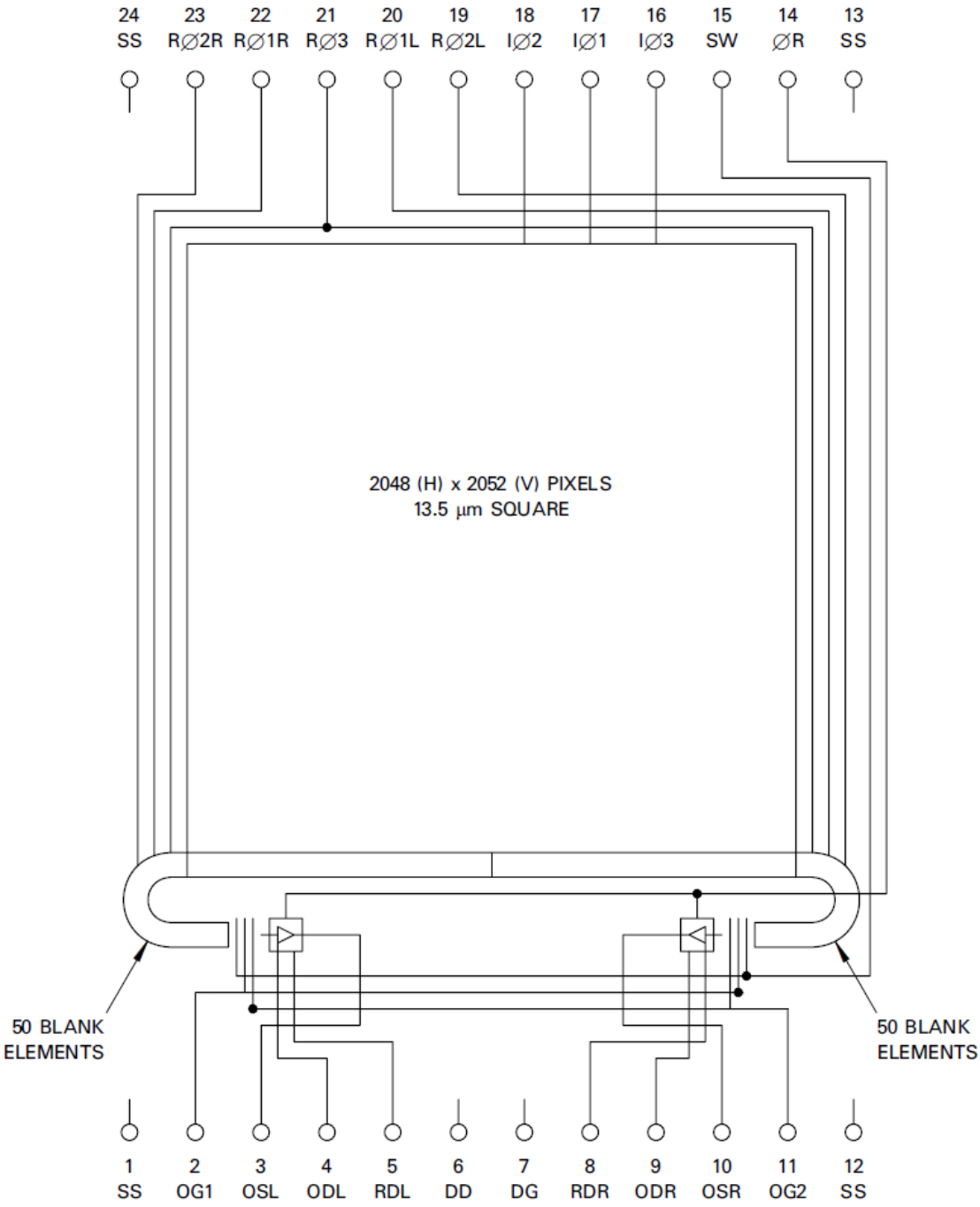
AIMO



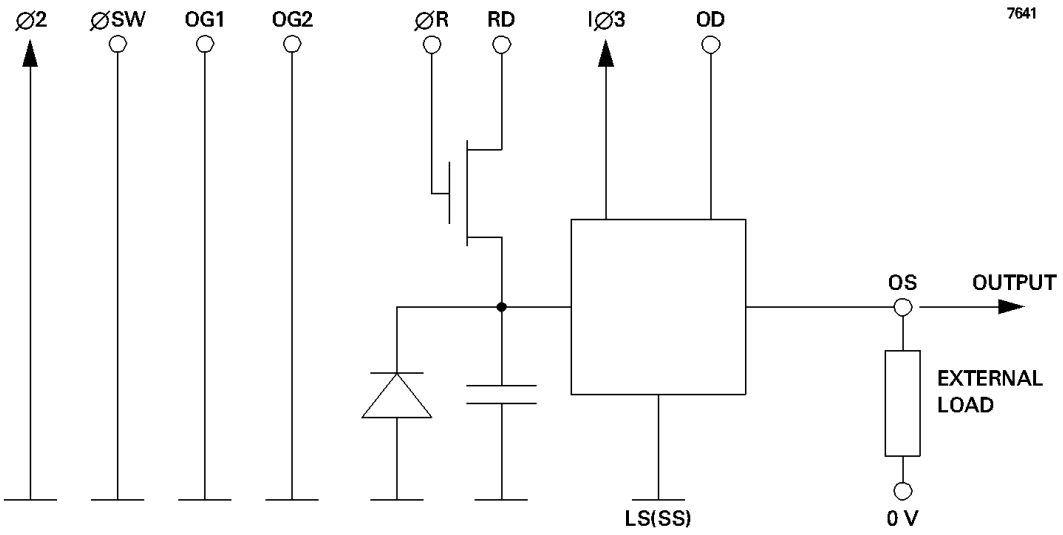
TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE



DEVICE SCHEMATIC



OUTPUT CIRCUIT



NOTES

13. The amplifier has a DC restoration circuit which is internally activated whenever I∅3 is high.
14. External load not critical; can be a 3 to 5 mA constant current supply or an appropriate load resistor.

CONNECTIONS TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

NIMO

PIN	REF	DESCRIPTION	CLOCK LOW Typical	CLOCK HIGH OR DC LEVEL (V)			MAXIMUM RATINGS with respect to V_{SS}
				Min	Typical	Max	
1	SS	Substrate (see note 15)	n/a	0	9	10	-
2	OG1	Output gate 1	n/a	2	3	4	±20 V
3	OSL	Output transistor source (left)	n/a	see note 16			–0.3 to +25 V
4	ODL	Output drain (left)	n/a	27	29	31	–0.3 to +32 V
5	RDL	Reset drain (left)	n/a	15	17	19	–0.3 to +25 V
6	DD	Dump drain	n/a	22	24	26	–0.3 to +30 V
7	DG	Dump gate (see note 17)	0	-	12	15	±20 V
8	RDR	Reset drain (right)	n/a	15	17	19	–0.3 to +25 V
9	ODR	Output drain (right)	n/a	27	29	31	–0.3 to +32 V
10	OSR	Output transistor source (right)	n/a	see note 16			–0.3 to +25 V
11	OG2	Output gate 2 (see note 18)	4	16	20	24	±25 V
12	SS	Substrate	n/a	0	9	10	-
13	SS	Substrate	n/a	0	9	10	-
14	∅R	Reset gate	0	8	12	15	±20 V
15	SW	Summing well		Clock as R∅3			±20 V
16	I∅3	Image area clock, phase 3	0	8	10	15	±20 V
17	I∅1	Image area clock, phase 1	0	8	10	15	±20 V
18	I∅2	Image area clock, phase 2	0	8	10	15	±20 V
19	R∅2L	Register clock phase 2 (left)	1	8	11	15	±20 V
20	R∅1L	Register clock phase 1 (left)	1	8	11	15	±20 V
21	R∅3	Register clock phase 3	1	8	11	15	±20 V
22	R∅1R	Register clock phase 1 (right)	1	8	11	15	±20 V
23	R∅2R	Register clock phase 2 (right)	1	8	11	15	±20 V
24	SS	Substrate	n/a	0	9	10	-

AIMO

PIN	REF	DESCRIPTION	CLOCK LOW Typical	CLOCK HIGH OR DC LEVEL (V)			MAXIMUM RATINGS with respect to V_{SS}
				Min	Typical	Max	
1	SS	Substrate	n/a	8	9.5	11	-
2	OG1	Output gate 1	n/a	2	3	4	±20 V
3	OSL	Output transistor source (left)	n/a	see note 16			–0.3 to +25 V
4	ODL	Output drain (left)	n/a	27	29	31	–0.3 to +32 V
5	RDL	Reset drain (left)	n/a	15	17	19	–0.3 to +25 V
6	DD	Dump drain	n/a	22	24	26	–0.3 to +30 V
7	DG	Dump gate (see note 17)	0	-	12	15	±20 V
8	RDR	Reset drain (right)	n/a	15	17	19	–0.3 to +25 V
9	ODR	Output drain (right)	n/a	27	29	31	–0.3 to +32 V
10	OSR	Output transistor source (right)	n/a	see note 16			–0.3 to +25 V
11	OG2	Output gate 2 (see note 18)	4	16	20	24	±25 V
12	SS	Substrate	n/a	8	9.5	11	-
13	SS	Substrate	n/a	8	9.5	11	-
14	∅R	Reset gate	0	8	12	15	±20 V
15	SW	Summing well		Clock as R∅3			±20 V
16	I∅3	Image area clock, phase 3	0	8	15	16	±20 V
17	I∅1	Image area clock, phase 1	0	8	15	16	±20 V
18	I∅2	Image area clock, phase 2	0	8	15	16	±20 V
19	R∅2L	Register clock phase 2 (left)	1	8	11	15	±20 V
20	R∅1L	Register clock phase 1 (left)	1	8	11	15	±20 V
21	R∅3	Register clock phase 3	1	8	11	15	±20 V
22	R∅1R	Register clock phase 1 (right)	1	8	11	15	±20 V
23	R∅2R	Register clock phase 2 (right)	1	8	11	15	±20 V
24	SS	Substrate	n/a	8	9.5	11	-

If all voltages are set to the typical values, operation at or close to specification should be obtained. Some adjustment within the range specified may be required to optimise performance. Refer to the specific device test data if possible.

Maximum voltages between pairs of pins:
pin 3 (OSL) to pin 4 (ODL) ..... +15 V
pin 9 (ODR) to pin 10 (OSR) ..... +15 V
Maximum output transistor current..... 10 mA

NOTES

15. Standard silicon variants are tested with high substrate (9 V). Deep depleted variants are tested colder and with lo substrate (3V).
16. Not critical; OS = 3 to 5 V below OD typically. Connect to ground using a 3 to 5 mA current source or appropriate load resistor (typically 5 to 10 kΩ).
17. This gate is normally low. It should be pulsed high for charge dump.
18. OG2 = OG1 + 1 V for operation of the output in high responsivity, low noise mode. For operation at low responsivity, high signal, OG2 should be set high.
19. With the R∅ connections shown, the device will operate through both outputs simultaneously. In order to operate from the left output only, R∅1(R) and R∅2(R) should be reversed.

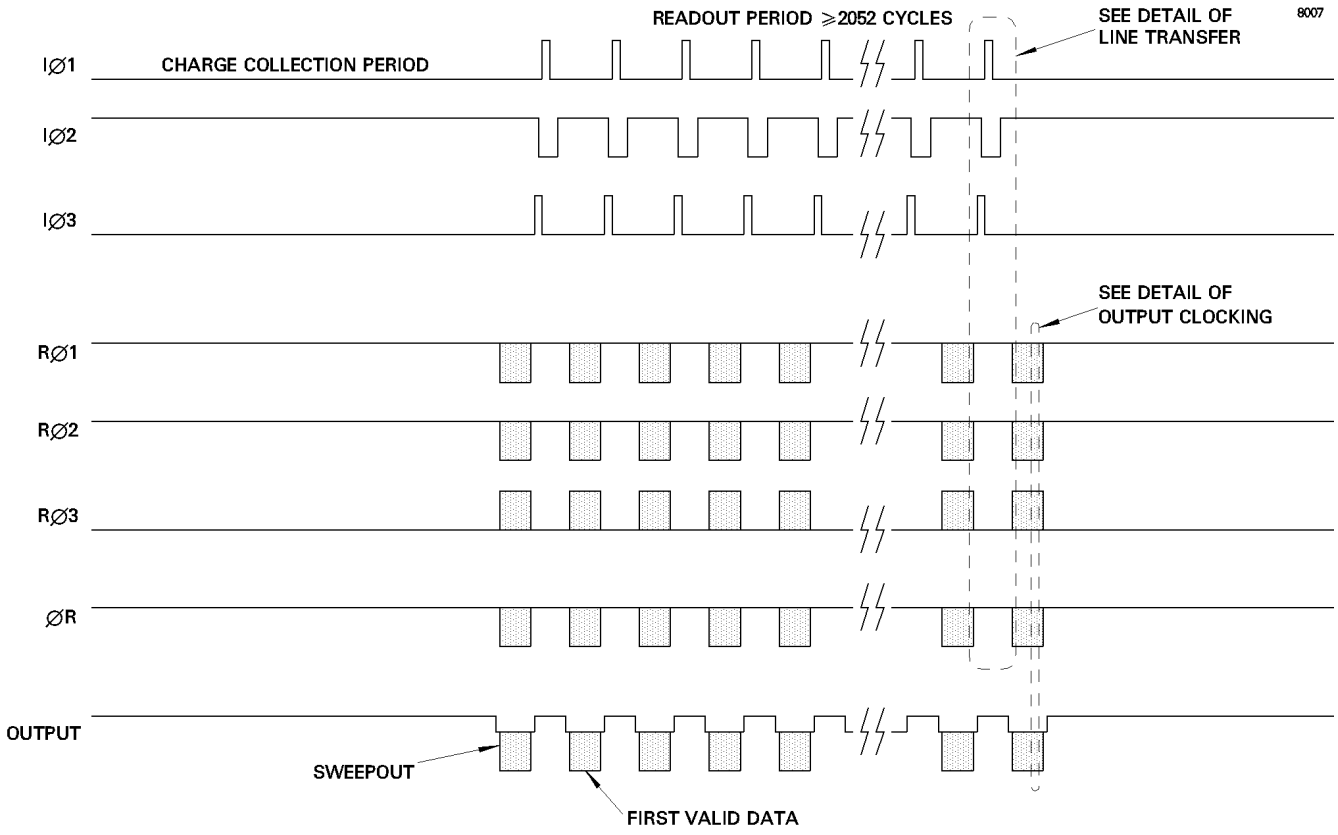
ELECTRICAL INTERFACE CHARACTERISTICS

Electrode Capacitances (Measured at mid-clock level)

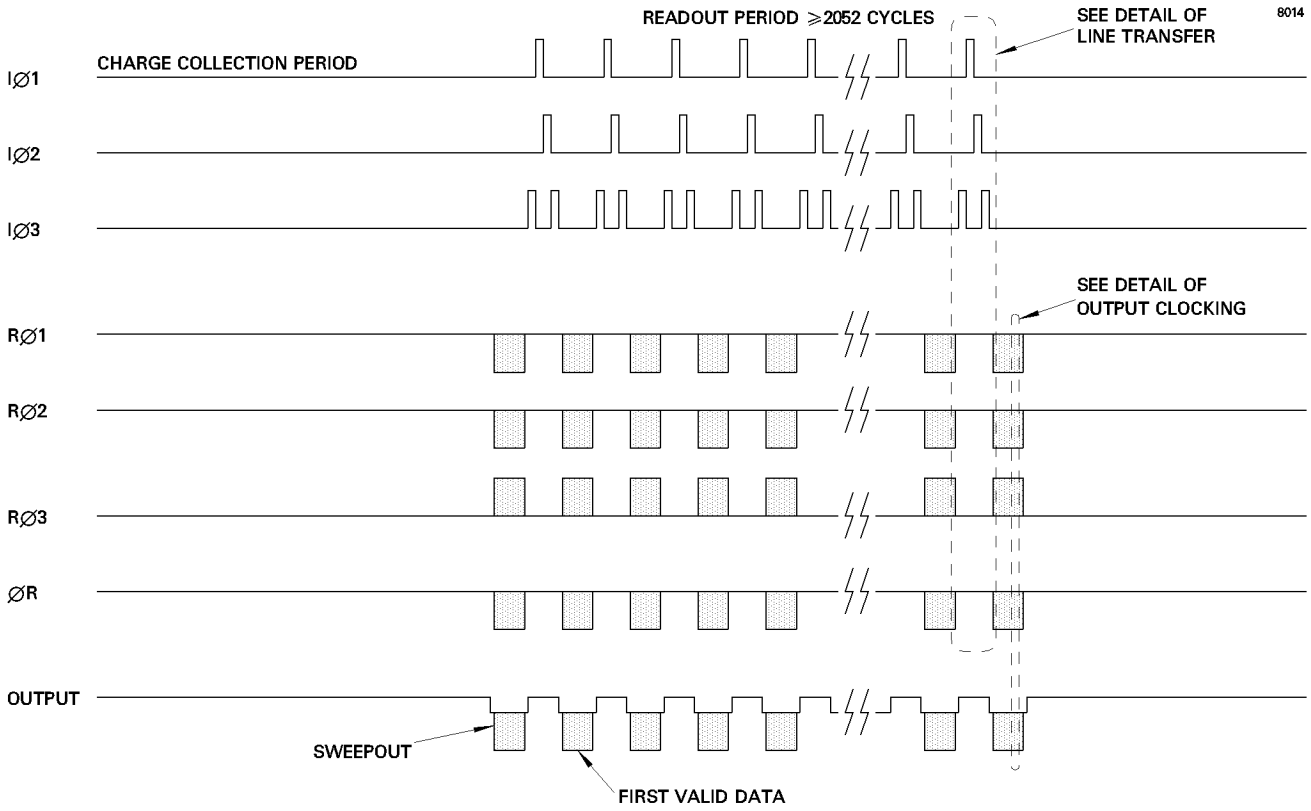
	Typical	Units
IØ/IØ interphase NIMO	16	nF
IØ/IØ interphase AIMO	18	nF
IØ/SS NIMO	32	nF
IØ/SSV AIMO	33	nF
RØ/RØ interphase	80	pF
RØ/(SS + DG + OD)	150	pF
Output impedance at typical operating conditions	350	Ω

FRAME READOUT TIMING DIAGRAM

NIMO

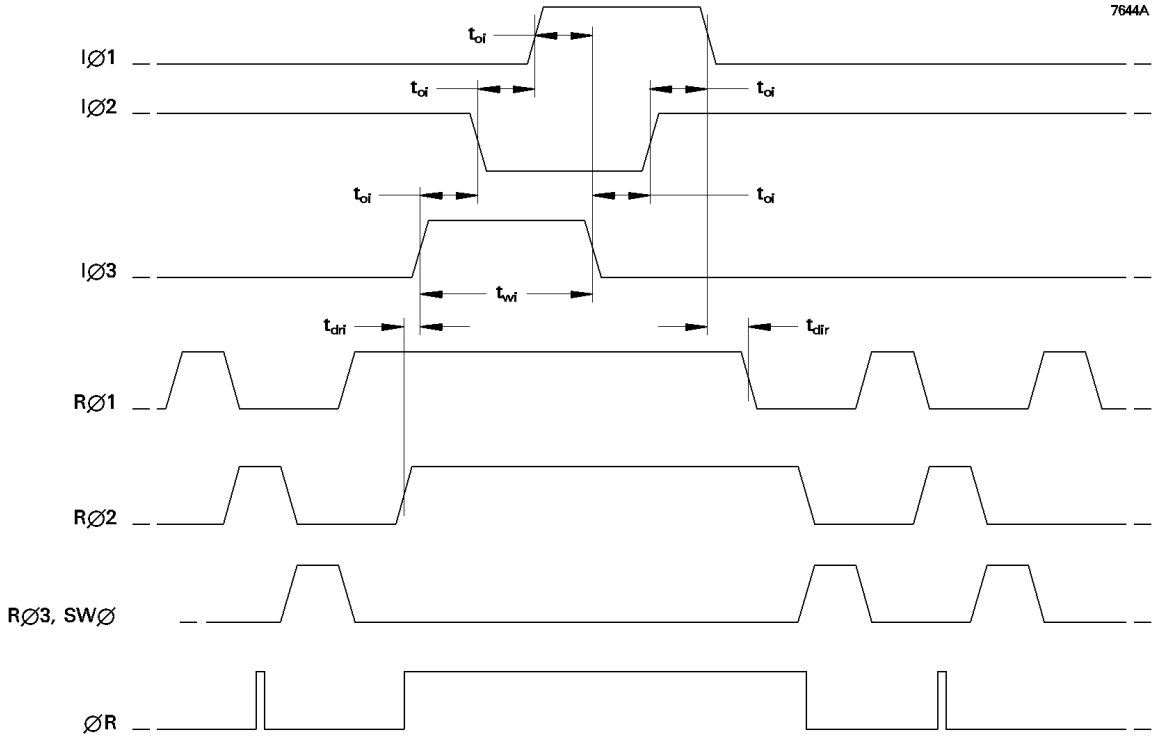


AIMO


READOUT PERIOD ⩾2052 CYCLES
SEE DETAIL OF LINE TRANSFER
8014
CHARGE COLLECTION PERIOD
IØ1
IØ2
IØ3
SEE DETAIL OF OUTPUT CLOCKING
RØ1
RØ2
RØ3
ØR
OUTPUT
SWEEPOUT
FIRST VALID DATA

DETAIL OF LINE TRANSFER (Not to scale)

NIMO



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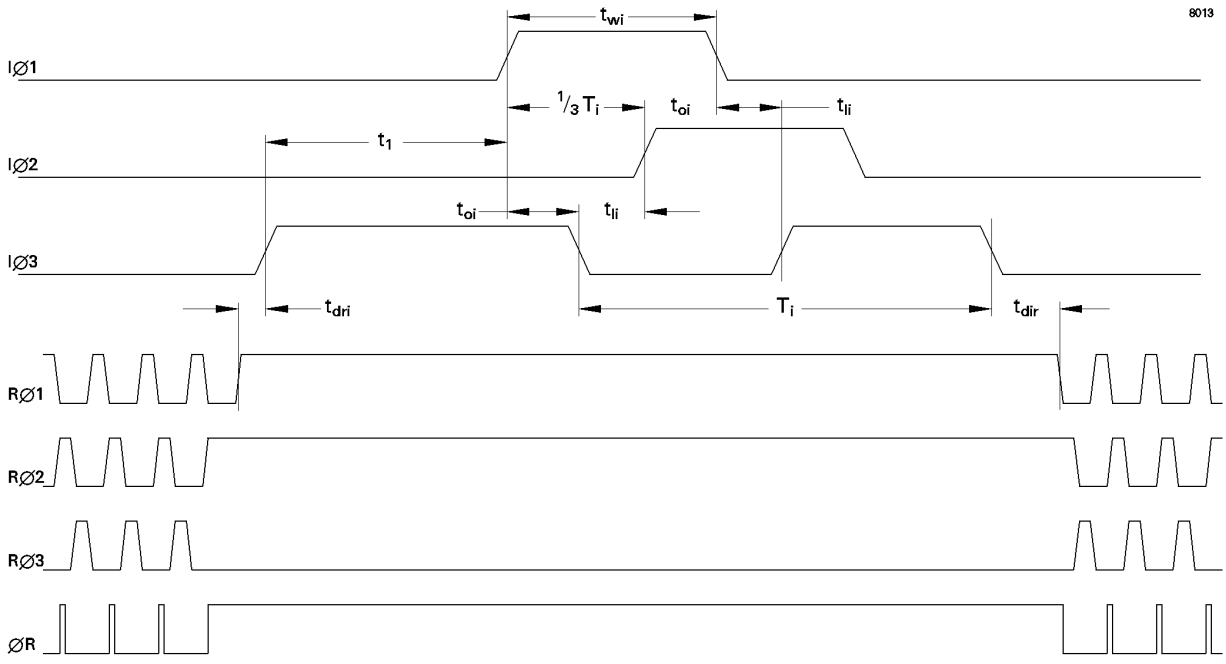
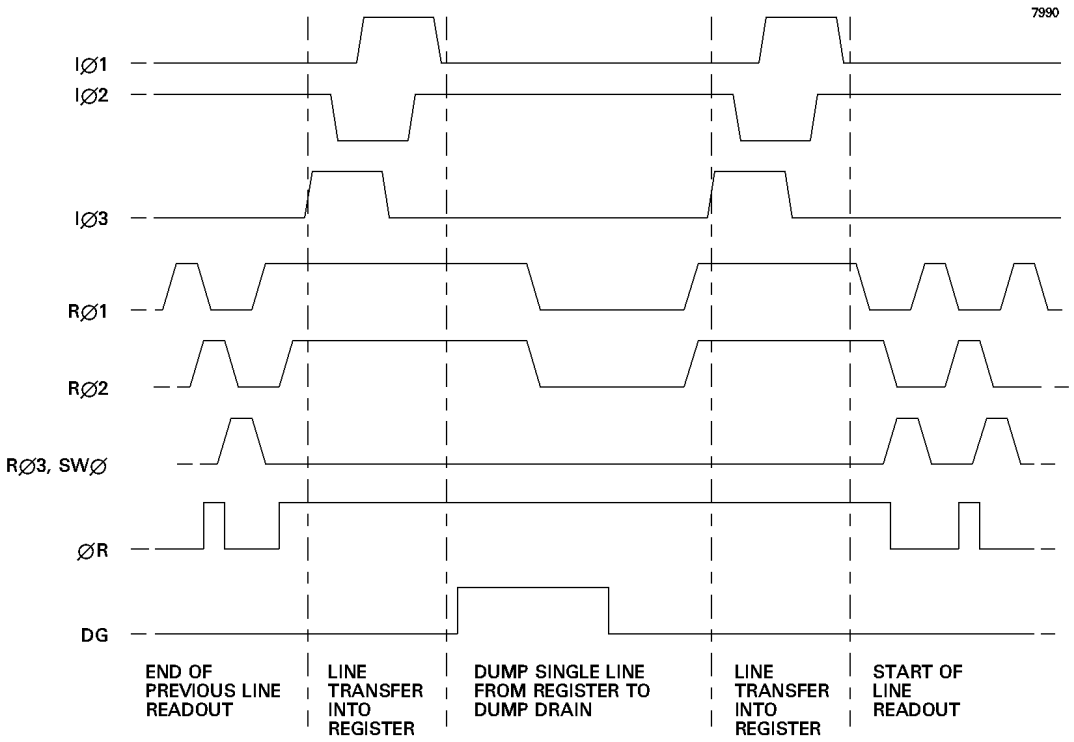


DETAIL OF VERTICAL LINE TRANSFER (Single line dump)

NIMO



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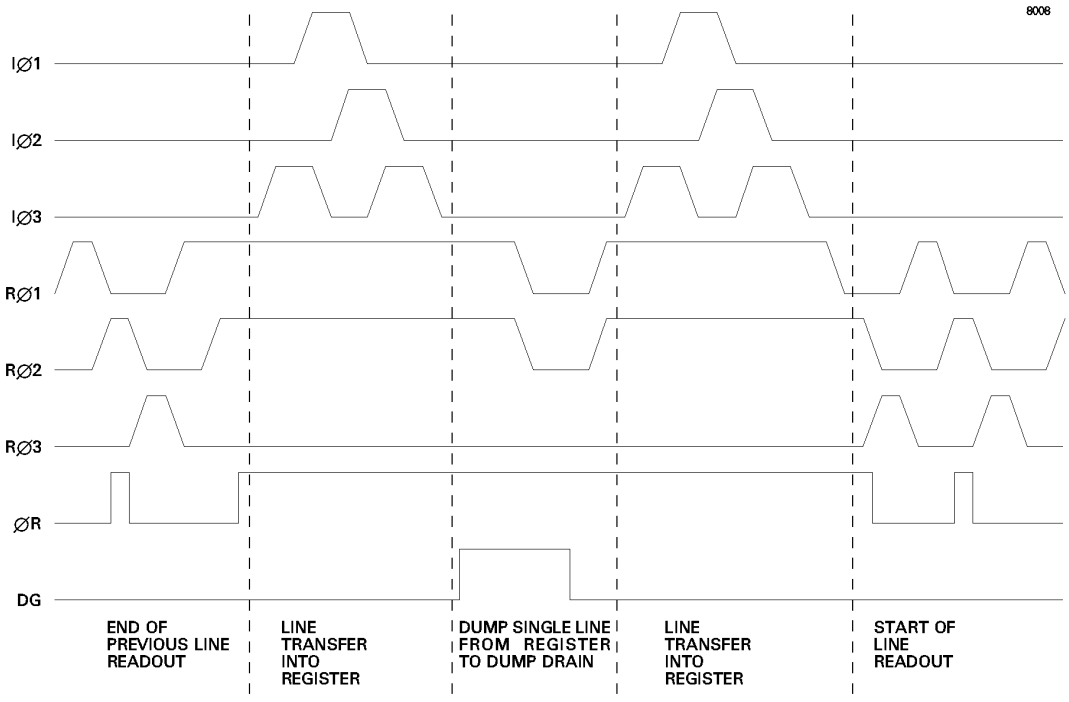
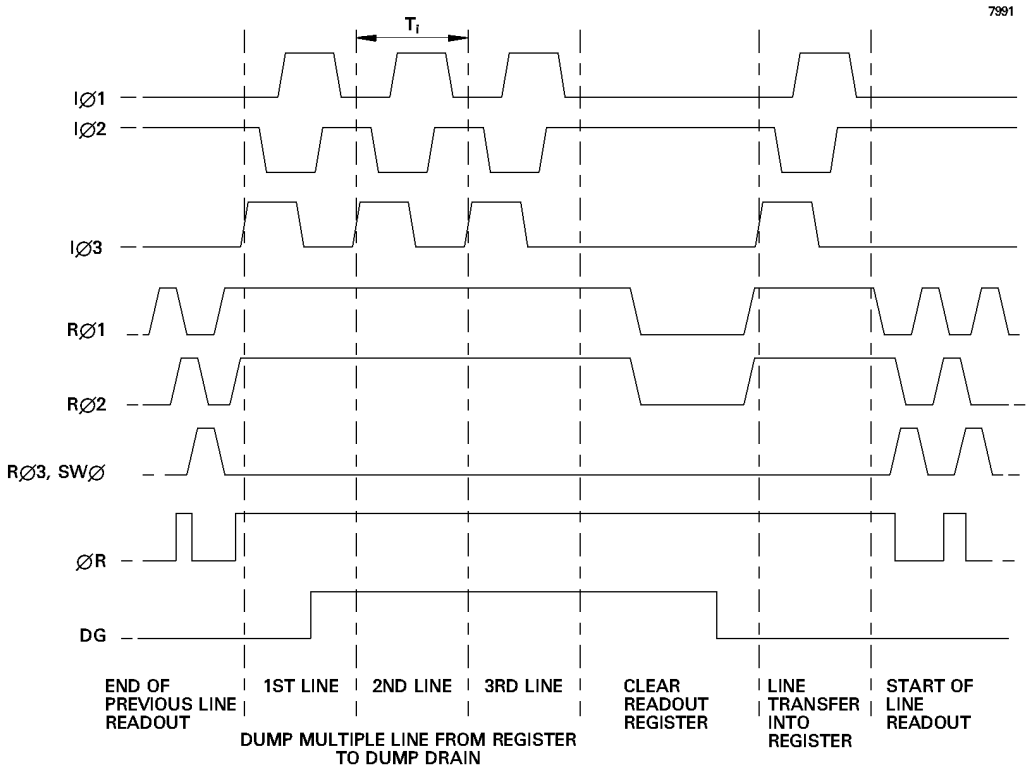
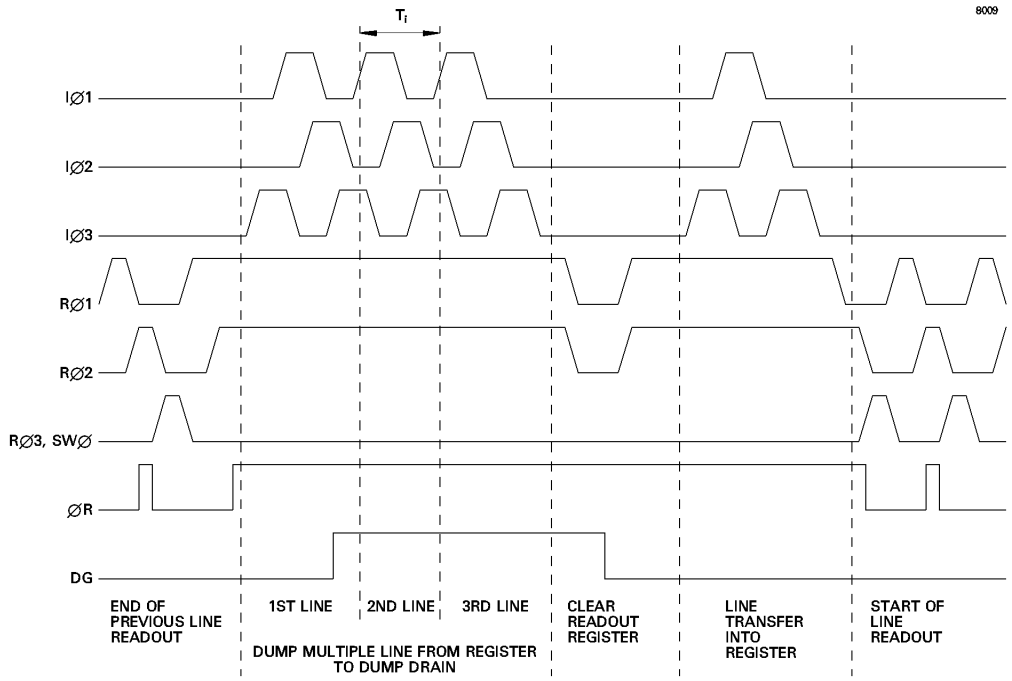


DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)

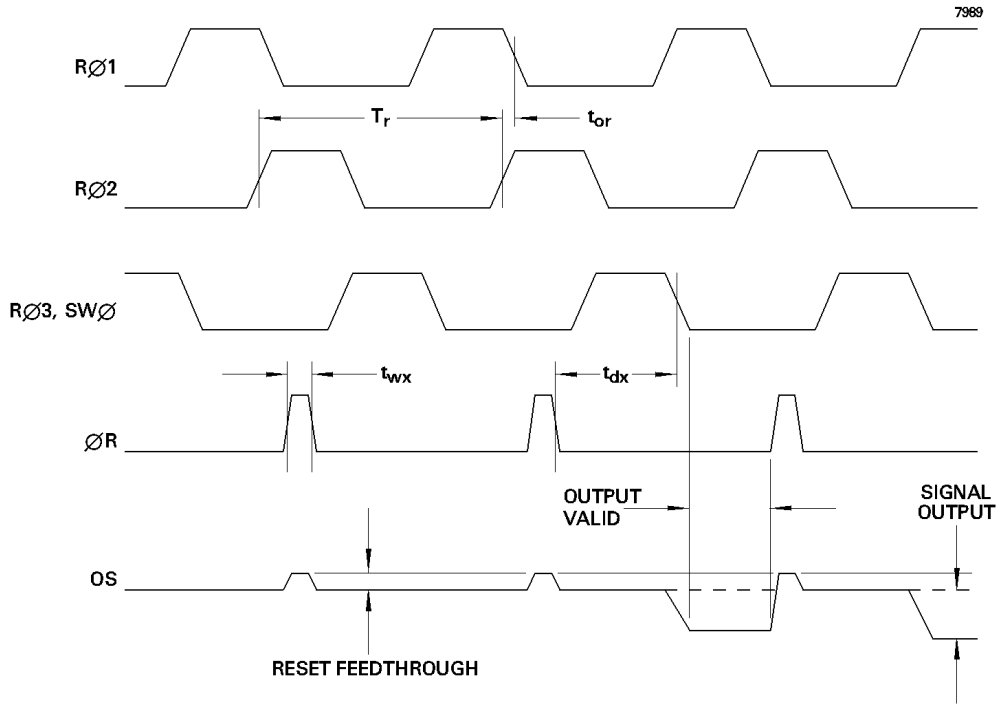
NIMO



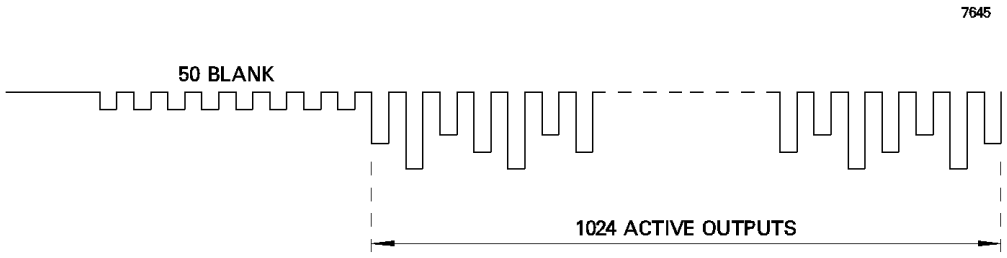
AIMO



DETAIL OF OUTPUT CLOCKING (Operation through both outputs)



LINE OUTPUT FORMAT (Split read-out operation)



CLOCK TIMING REQUIREMENTS

NIMO

Symbol	Description	Min	Typical	Max	Units
T_i•	Image clock period	10	20	see note 21	µs
t_{wi}	Image clock pulse width	5	10	see note 21	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	1	2	$0.2T_i$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	t_{ri}	$0.2T_i$	µs
t_{oi}	Image clock pulse overlap	$(t_{ri} + t_{fi})/2$	2	$0.2T_i$	µs
t_{dir}	Delay time, I∅ stop to R∅ start	3	5	see note 21	µs
t_{dri}	Delay time, R∅ stop to I∅ start	1	2	see note 21	µs
T_r	Output register clock cycle period	300	see note 22	see note 21	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ∅R low to R∅3 low	30	$0.5T_r$	$0.8T_r$	ns

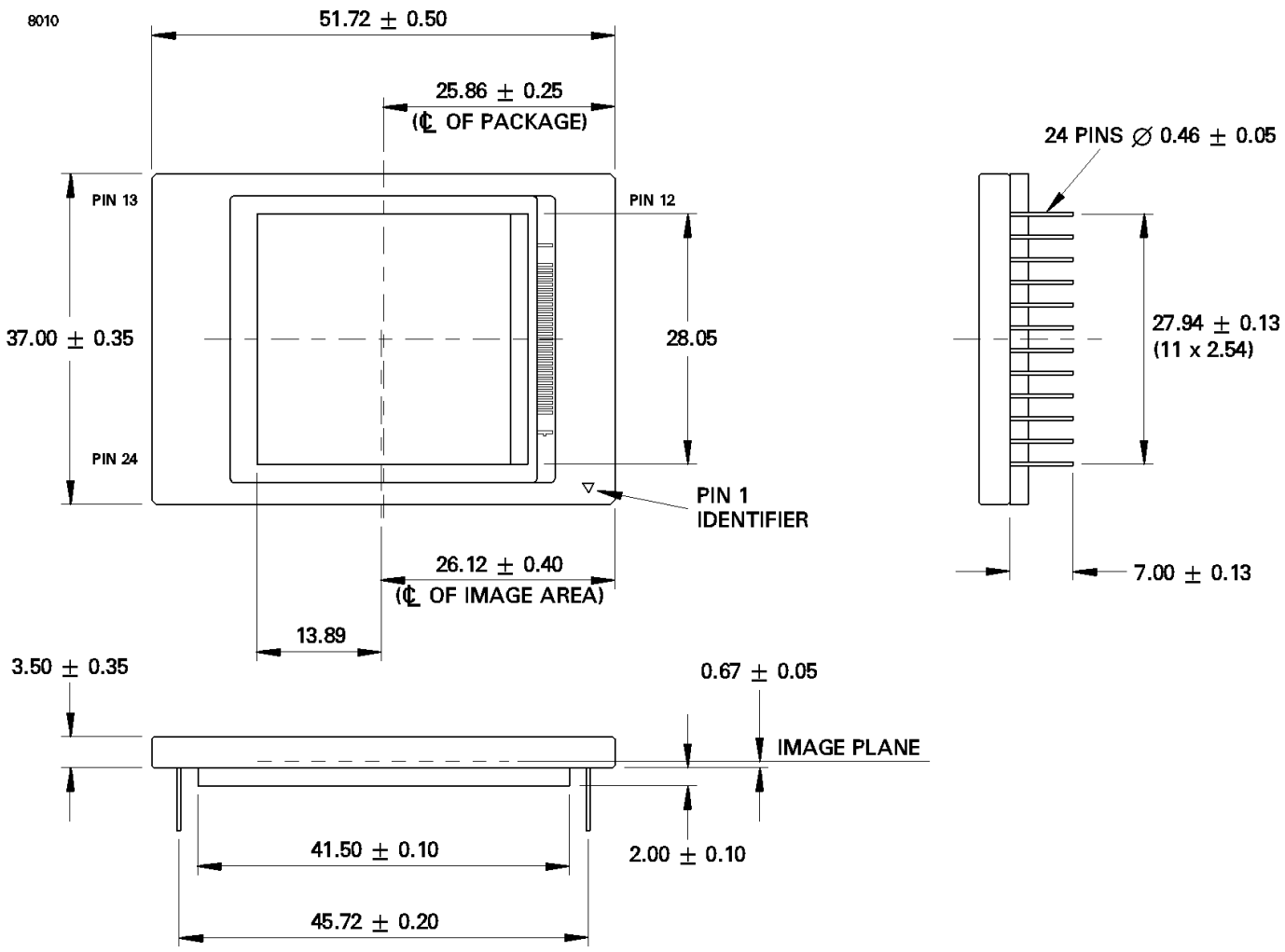
AIMO

Symbol	Description	Min	Typical	Max	Units
T_i•	Image clock period		100 (see note 20)	see note 21	µs
t_{wi}	Image clock pulse width		50 (see note 20)	see note 21	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	1	5	$0.2T_i$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	t_{ri}	$0.2T_i$	µs
t_{oi}	Image clock pulse overlap	$(t_{ri} + t_{fi})/2$	2	$0.2T_i$	µs
t_{dir}	Delay time, I∅ stop to R∅ start	3	5	see note 21	µs
t_{dri}	Delay time, R∅ stop to I∅ start	1	2	see note 21	µs
T_r	Output register clock cycle period	300	see note 22	see note 21	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ∅R low to R∅3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

20. The transfer of a line of charge in back-thinned AIMO devices is affected by a pile-up of the holes used to suppress dark current, as they cannot easily flow to and from the substrate connection when the clocks change state. This problem is eased by extending the t1 timing interval to 50 µs and/or the use of higher drive pulse amplitudes.
21. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
22. As set by the readout period.

OUTLINE (All dimensions in millimeters; dimensions without limits are nominal)



HEALTH AND SAFETY HAZARDS

Teledyne e2v devices are safe to handle and operate, provided that the relevant precautions stated herein are observed. Teledyne e2v does not accept responsibility for damage or injury resulting from the use of devices it produces. Equipment manufacturers and users must ensure that adequate precautions are taken. Appropriate warning labels and notices must be provided on equipment incorporating Teledyne e2v devices and in operating manuals.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 7, 11, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23) but not to the other pins.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising dose of greater than 10^4 rads.

Certain characterisation data are held at Teledyne e2v. Users planning to use CCDs in a high radiation environment are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	153	-	373	K
Operating NIMO	153	243	323	K
Operating AIMO	153	253	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling ..... 5 K/min

PART REFERENCES

Variant	Operating Mode	Illumination	Enhanced BSI Process	Silicon	AR Coating	Fringe Suppression
CCD42-40-G-368	AIMO	BSI	No	Standard	Midband	No
CCD42-40-G-385	AIMO	BSI	No	Standard	None	No
CCD42-40-G-075	NIMO	BSI	Yes	Standard	UV	No
CCD42-40-G-114	NIMO	BSI	Yes	Standard	Broadband	No
CCD42-40-G-115	NIMO	BSI	No	Deep Depletion	NIR	No
CCD42-40-G-140	NIMO	BSI	Yes	Standard	None	No
CCD42-40-G-169	NIMO	BSI	No	Deep Depletion	NIR	Yes
CCD42-40-G-S04	NIMO	BSI	Yes	Deep Depletion	Multi-2	Yes
CCD42-40-G-S06	NIMO	BSI	No	Deep Depletion	None	Yes

Grade Definitions

Grade 0	Super Grade	Meets all performance parameters and Grade 0 cosmetic parameters
Grade 1	Science Grade	Meets all performance parameters and Grade 1 cosmetic parameters
Grade 5	Engineering Grade	Electrically functional with no performance or cosmetic parameter guarantees
Grade 6	Mechanical Grade	Non-functional. Mechanically representative only.

NOTES

23. G = Grade (e.g. 1)
24. Additional variants may be available to custom order. Consult Teledyne e2v for more information.