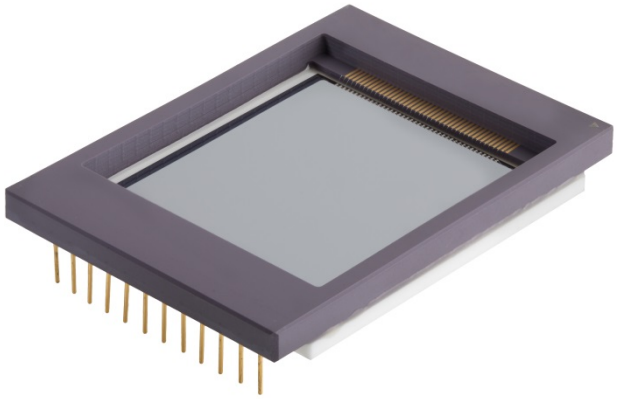
CCD42-40 Ceramic AIMO Front Illuminated Large Area Sensor for Scientific Applications

MAIN FEATURES

- 2048 by 2048 active pixels
- 13.5µm square pixels
- Advanced inverted mode operation (AIMO)
- Low Noise Output Amplifier
- Dual Responsivity Output
- Full-frame Architecture
- Gated Dump Drain on Output Register
- Compact Footprint Ceramic Package



OVERVIEW

This version of the CCD42 family of CCD sensors has full-frame architecture, which in combination with extremely low noise amplifier, makes the device well suited for use in general scientific imaging. The advanced inverted mode operation (AIMO) gives a 100-times reduction in dark current with minimal full-well reduction and is suitable for use at Peltier temperatures.

The output amplifier is designed to give excellent noise levels at low pixel rates and can match the noise performance of most conventional science CCDs at pixel rates as high as 3 MHz.

There are two low noise amplifiers in the readout register, one at each end. Charge can be made to transfer through either or both amplifiers by making the appropriate R∅ connections. The readout register has a gate controlled dump drain to allow fast dumping of unwanted data.

The register is designed to accommodate four image pixels of charge and a summing well is provided capable of holding six image pixels of charge. The output amplifier has a feature to enable the responsivity to be reduced, allowing the reading of such large charge packets.

GENERAL DATA

Active pixels	2048 (H) 2048+4 (V)
Pixel size	13.5 × 13.5 µm
Active image area	27.6 × 27.6 mm
Package size	37.0 × 51.7 mm
Number of output amplifiers	2
Number of underscan (serial) pixels	50
Typical amplifier responsivity	4.5 µV/e^-
Typical readout noise @ 20 kHz	3 e- rms
Maximum readout frequency	3 MHz
Typical pixel charge capacity	100 ke^-/pixel
Typical dark signal (20°C)	100 e^-/pixel/s

ORDERING INFORMATION

CCD42-40-G-XYZ
G = cosmetic grade
XYZ = specific variant type (e.g. AR coating)
e.g. XYZ = 383 for front-illuminated AIMO

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IMAGING PERFORMANCE

ELECTRO-OPTICAL PERFORMANCE

Parameter	Min	Typical	Max	Units	Note
Peak charge storage	80k	100k		e^-/pixel	note 1
Peak output voltage (unbinned)		450		mV	
Dark signal at 293 K		100	200	e^-/pixel/s	note 2
Dark Signal Non Uniformity at 293 K (std. deviation)		40	80	e^-/pixel/s	
Charge transfer efficiency (Parallel)	99.999	99.9999	-	%	note 3
Charge transfer efficiency (Series)	99.999	99.9993	-	%	
Output amplifier responsivity (Low noise mode)	3.0	4.5	6.0	µV/e^-	
Output amplifier responsivity (High signal mode)		1.5			
Readout noise at 253 K		3.0	4.0	rms e^-/pixel	note 4
Readout frequency		20	3000	kHz	note 5
Output node capacity		1,000,000		e^-	note 6

ELECTRICAL INTERFACE CHARACTERISTICS

Typical Electrode Capacitances At Mid-Clock Level (Not Measured)

	Min	Typical	Max	Units
IØ/IØ interphase	-	18	-	nF
IØ/SS	-	33	-	nF
RØ/RØ interphase	-	80	-	pF
RØ/(SS + DG + OD)	-	150	-	pF
Output impedance at typical operating conditions	-	350	-	Ω

Notes

1. Signal level at which resolution begins to degrade.
2. The typical average (background) dark signal at any temperature T (Kelvin) between 230 K and 300K is given by:

$$Q_d/Q_{d0} = 1.14 \times 10^6 T^3 e^{-9080/T}$$

   where Q_{d0} is the dark signal at 293 K. Below 230 K additional dark current components with a weaker temperature dependence may become significant.
3. CTE is measured for a complete 3-phase clock triplet at 173 K.
4. Measured using correlated double sampling. Noise specification applies to 20 kHz in low noise mode.
5. Readout above 3 MHz can be achieved but performance to the parameters given cannot be guaranteed.
6. With output circuit configured in low responsivity/high signal mode (OG2 high). This mode is not factory tested.

DEFECT DEFINITIONS

Parameter	Grade 0	Grade 1	Definition
Traps	10	20	Traps are pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e- at 253K.
Black Spots	50	75	Black spots are defined as having a signal less than 90% of the local mean at a signal level of approximately half full-well.
White Spots	50	75	White spots are defined as having a dark signal generation rate 125 times the maximum specified. The typical temperature dependence of white spots is given by: $Q_d/Q_{do} = 122T^3e^{-6400/T}$
Column Defects; Black or White	0	1	A column defect contains at least 21 black or 21 white defects.

Grade 5 devices are functional but with an image quality below grade 1. Other specifications may also not be met or may not have been tested.

The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 253 K. The amplitude of white spots and columns will decrease rapidly with temperature.

FIGURE 1: TYPICAL SPECTRAL RESPONSE (At -20°C, no window, standard thickness)

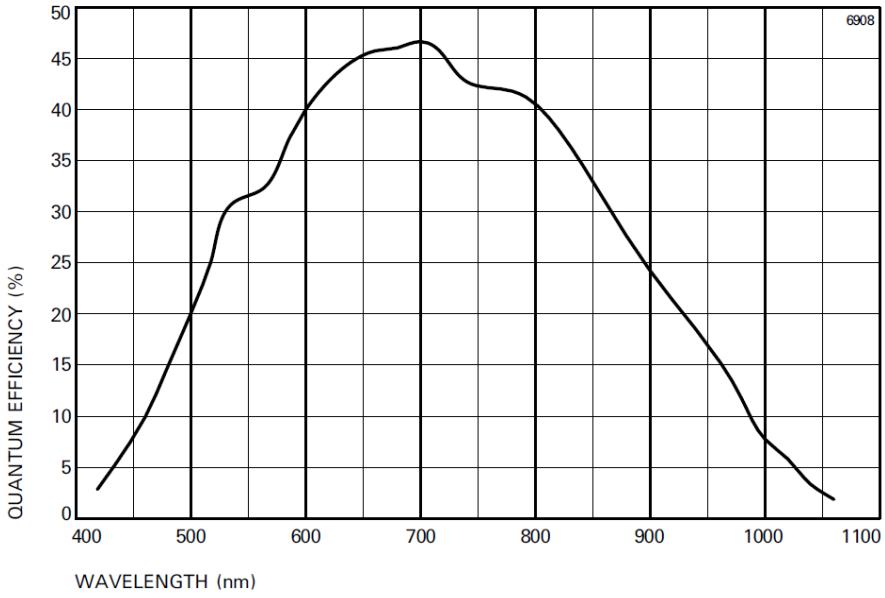


FIGURE 2: TYPICAL OUTPUT CIRCUIT NOISE (If Measured using clamp and sample)

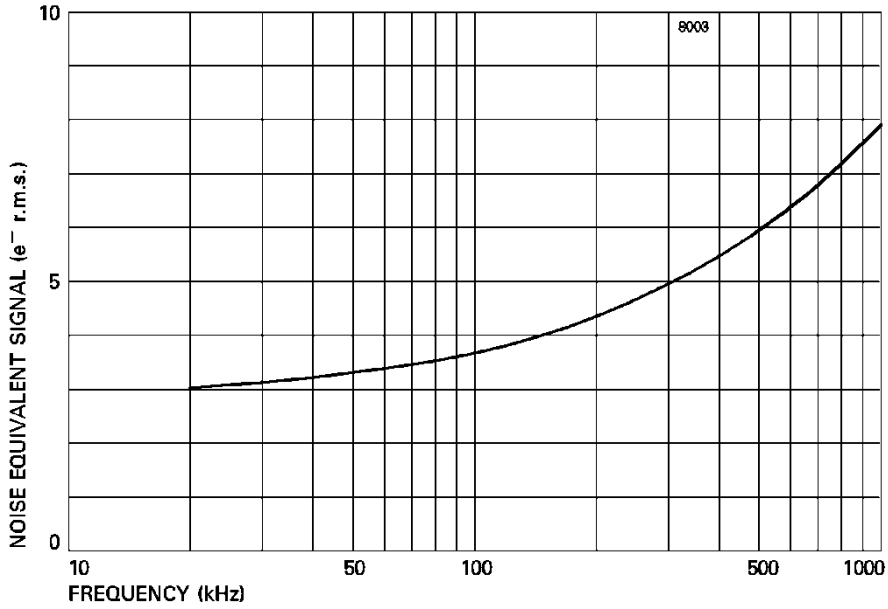


FIGURE 3: TYPICAL VARIATION OF DARK CURRENT WITH SUBSTRATE VOLTAGE AT 20 °C

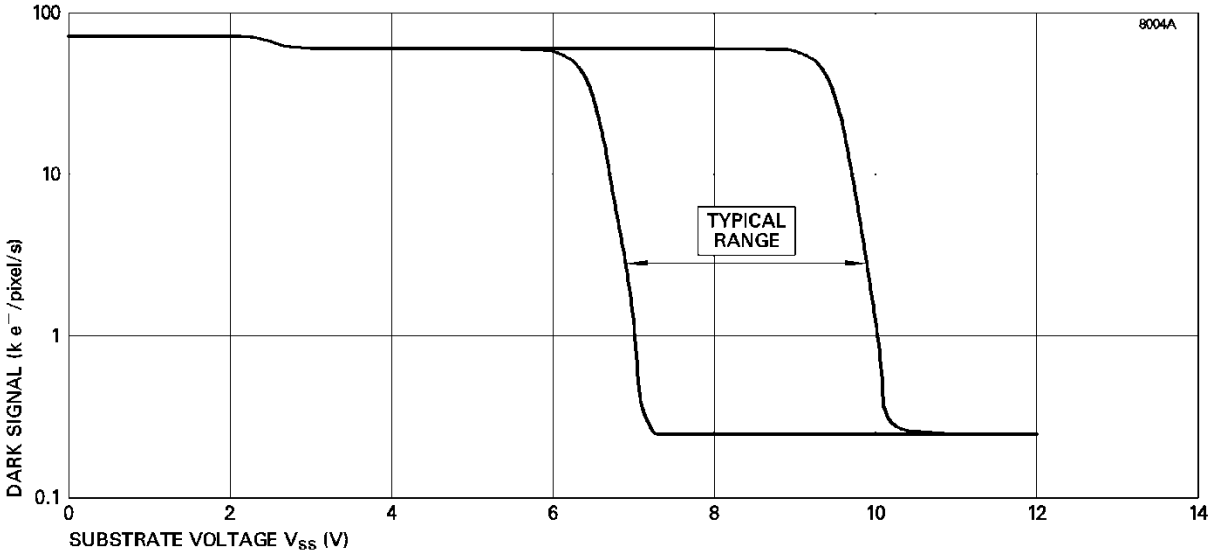


FIGURE 4: TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE

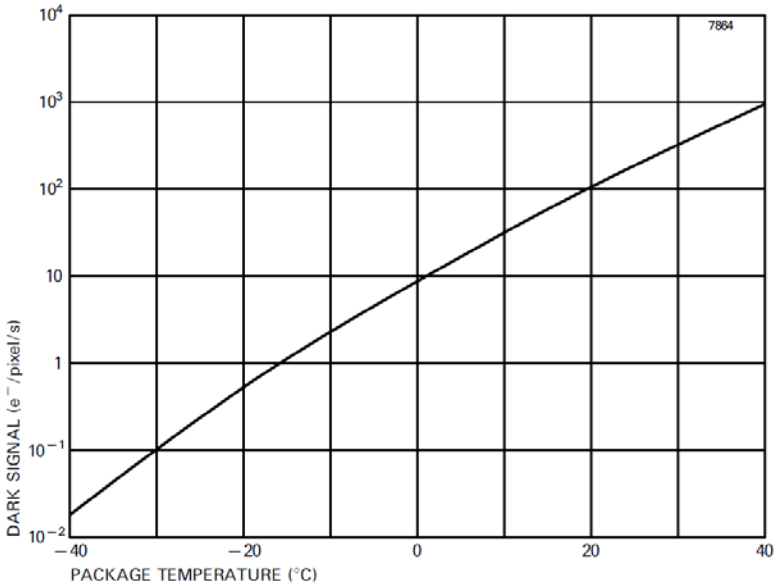
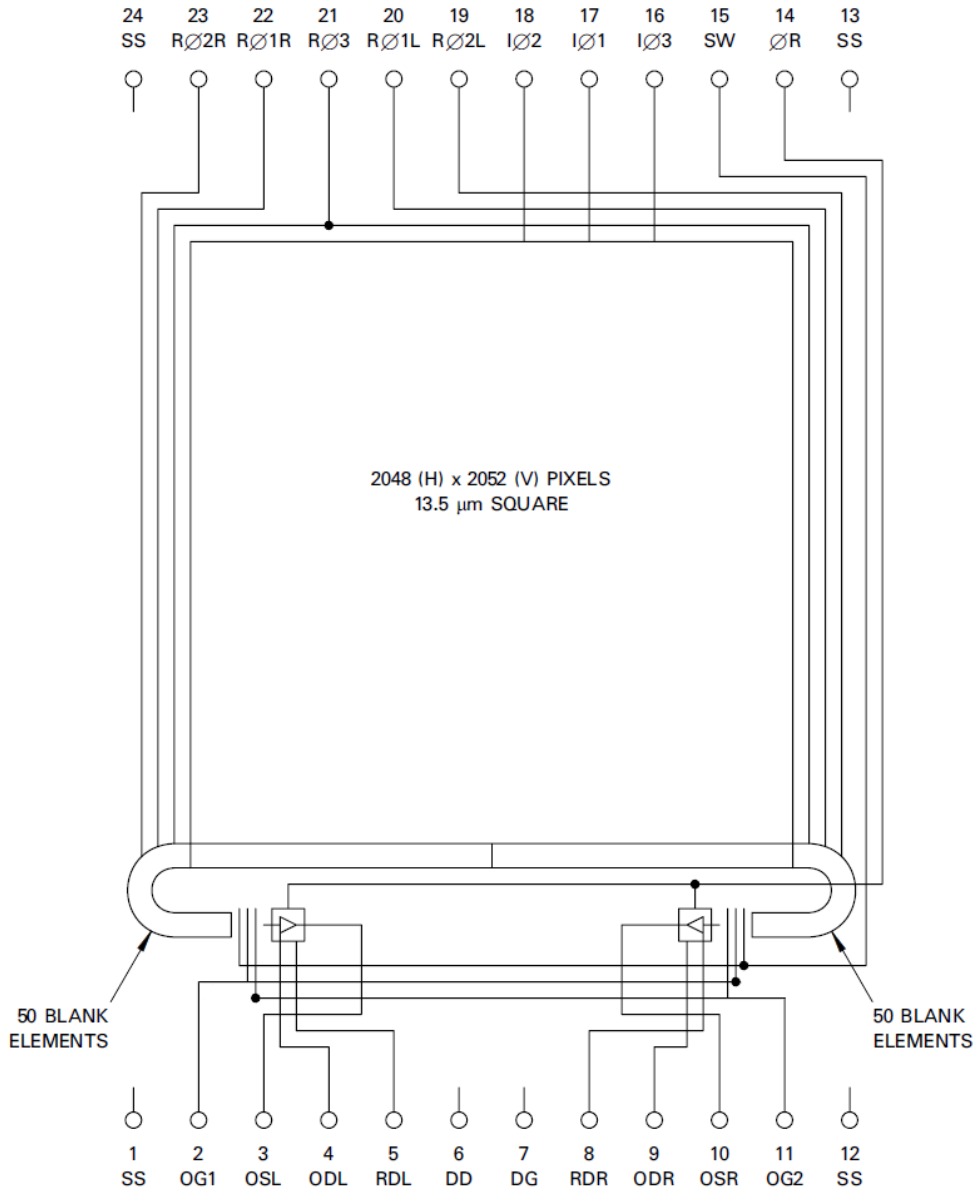


FIGURE 5: DEVICE SCHEMATIC



OPERATING VOLTAGES

PIN	REF	DESCRIPTION	TYPICAL VOLTAGE
1	SS	Substrate	9.5
2	OG1	Output gate 1	3
3	OSL	Output transistor source (left)	see note 8
4	ODL	Output drain (left)	31
5	RDL	Reset drain (left)	18
6	DD	Dump drain	24
7	DG	Dump gate (see note 9)	0
8	RDR	Reset drain (right)	18
9	ODR	Output drain (right)	31
10	OSR	Output transistor source (right)	see note 8
11	OG2	Output gate 2	see note 7
12	SS	Substrate	9.5
13	SS	Substrate	9.5
14	∅R	Reset gate	12
15	SW	Summing well	11
16	I∅3	Image area clock, phase 3	12
17	I∅1	Image area clock, phase 1	12
18	I∅2	Image area clock, phase 2	12
19	R∅2L	Register clock phase 2 (left)	11
20	R∅1L	Register clock phase 1 (left)	11
21	R∅3	Register clock phase 3	11
22	R∅1R	Register clock phase 1 (right)	11
23	R∅2R	Register clock phase 2 (right)	11
24	SS	Substrate	9.5

If all voltages are set to the typical values, operation at or close to specification should be obtained. Some adjustment within the range specified may be required to optimise performance. Refer to the specific device test data if possible.

Maximum Voltage Between Pairs

pin 3 (OSL) to pin 4 (ODL)..... +15 V
pin 9 (ODR) to pin 10 (OSR)..... +15 V
Maximum output transistor current .....10 mA

Notes

7. OG2 = OG1 + 1 V – normal low noise mode or OG2 = 20V – low responsivity/increased charge handling mode.
8. OS = 3 to 5 V below OD typically. Use 3 – 5 mA current source or 5 – 10 kΩ load.
9. Non-charge dumping level is shown. For charge dumping, DG should be pulsed to 12 ± 2 V.
10. Readout register clock pulse low levels +1 V; other clock low levels 0 ± 0.5 V.
11. With R∅ connections shown, this device will operate through both outputs. In order to operate from the left-hand output only, R∅1(R) and R∅2(R) should be reversed.

FIGURE 6: FRAME READOUT TIMING DIAGRAM

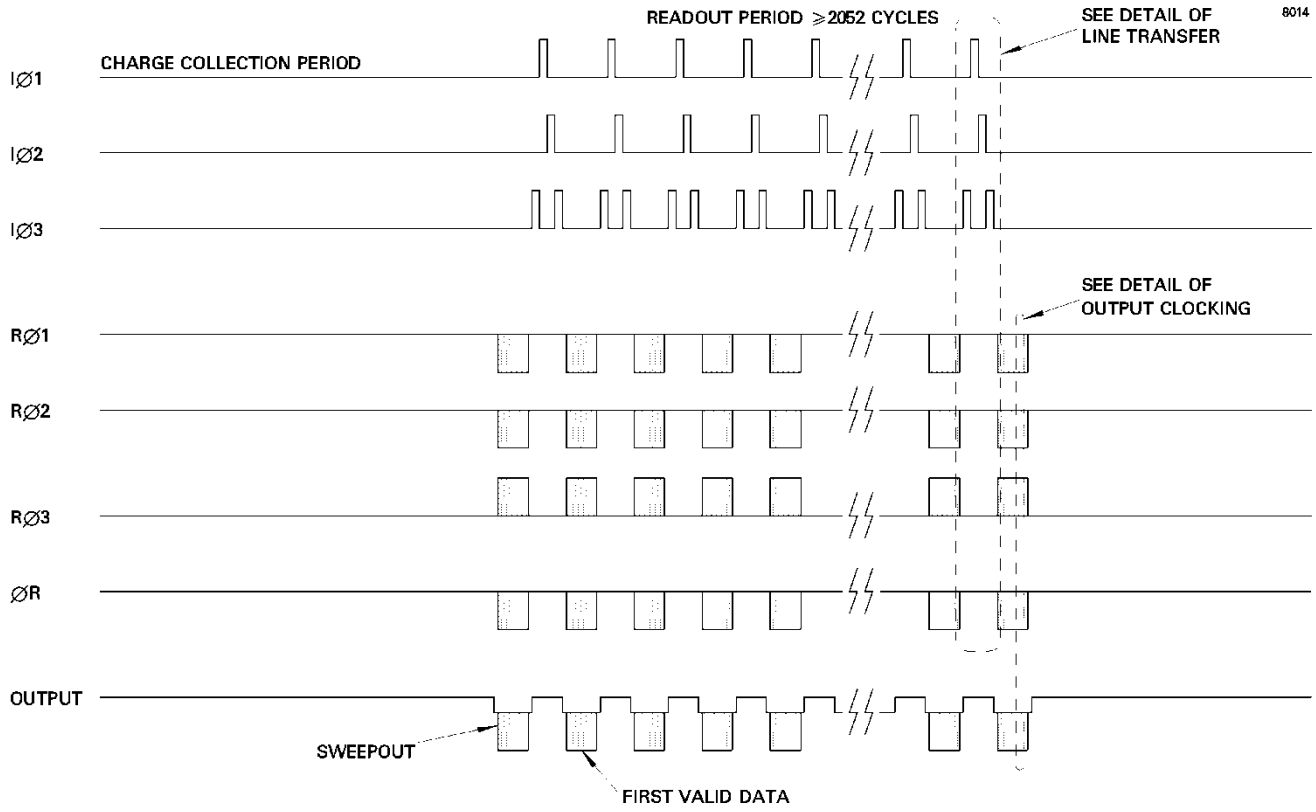


FIGURE 7: DETAIL OF LINE TRANSFER (Not to scale)

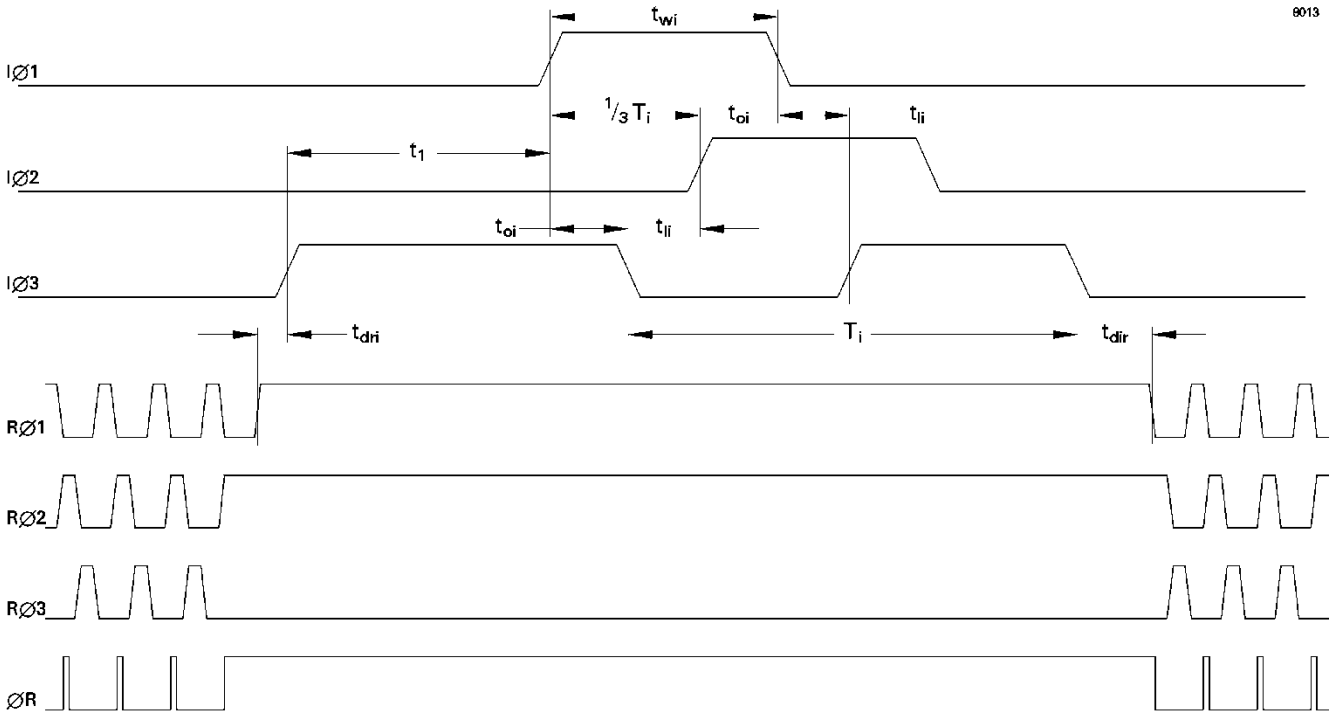


FIGURE 8: DETAIL OF VERTICAL LINE TRANSFER (Single line dump)

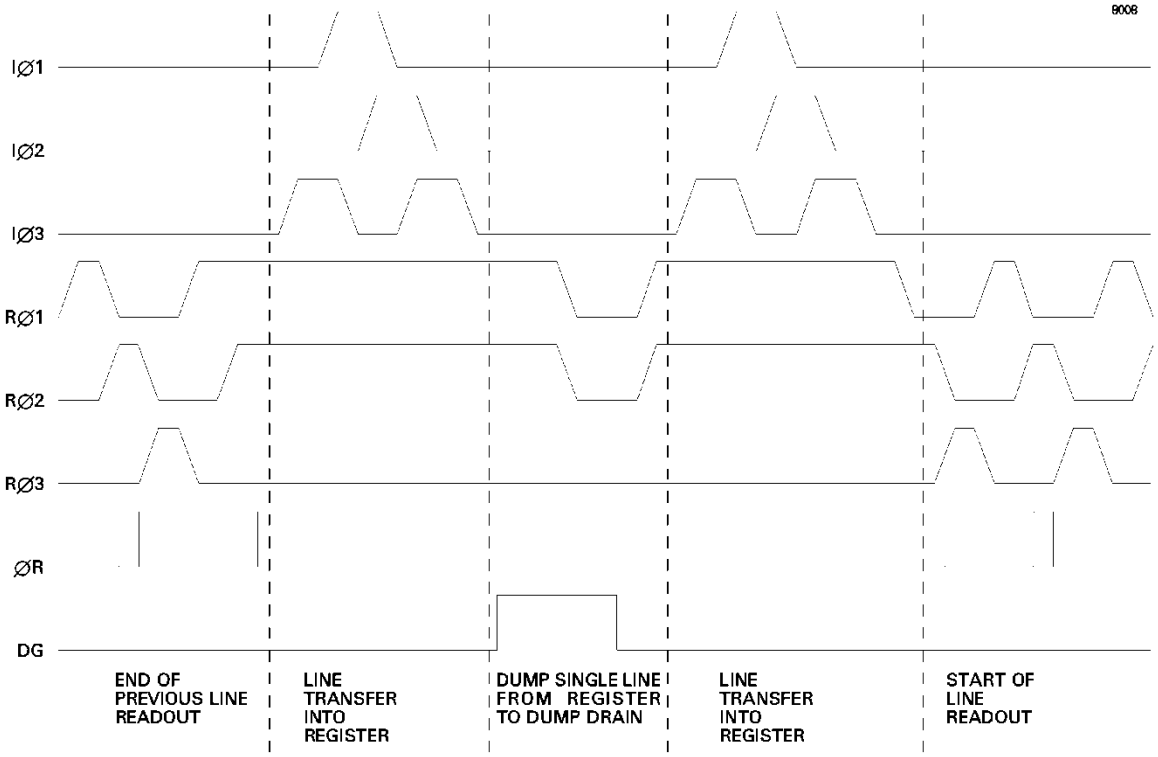


FIGURE 9: DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)

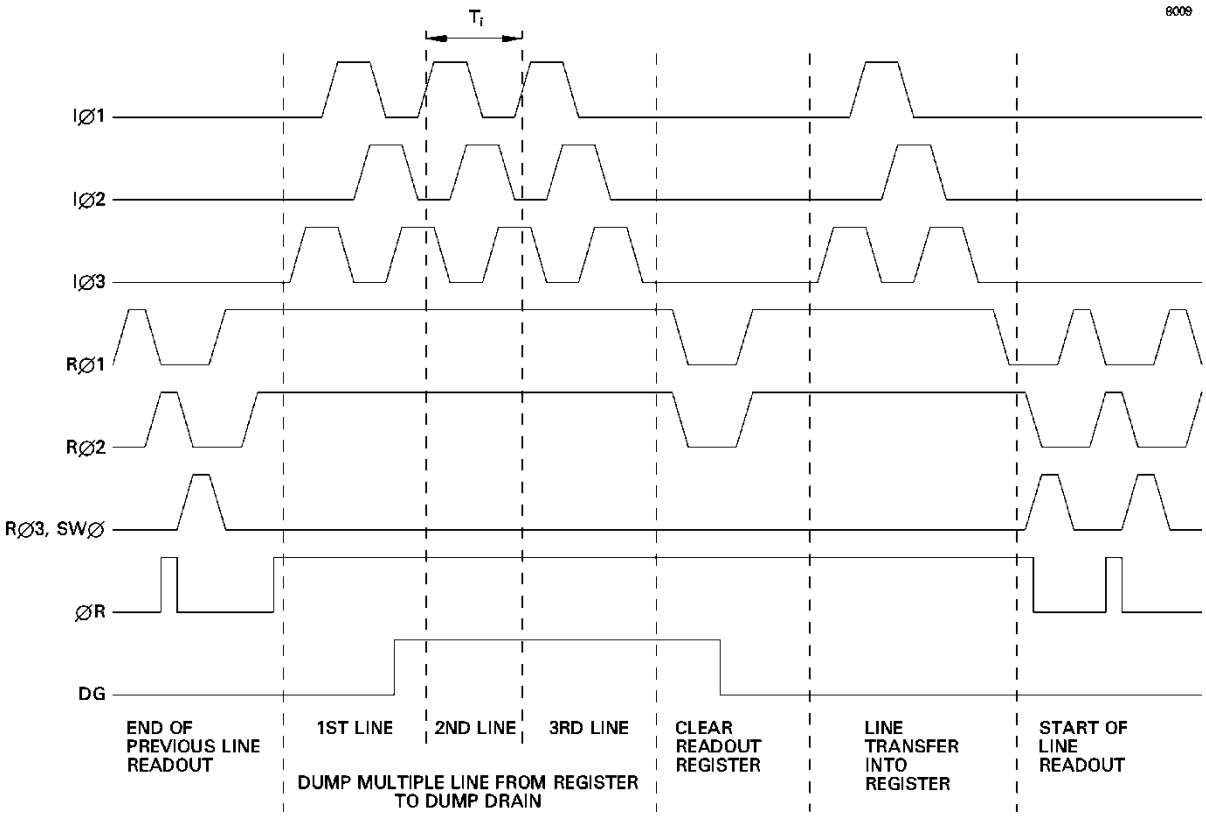


FIGURE 10: DETAIL OF OUTPUT CLOCKING (Operation through both outputs)

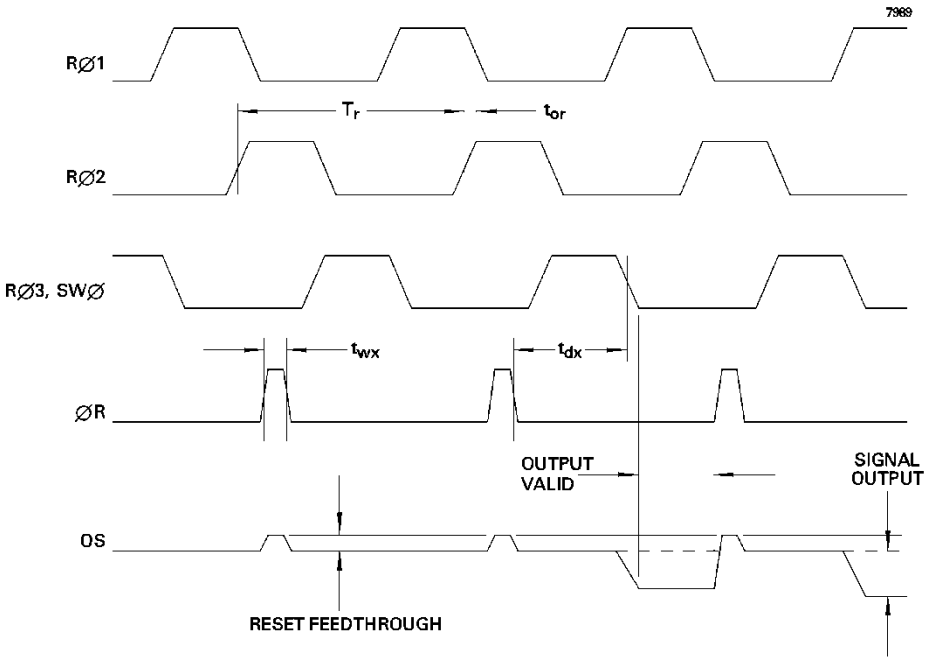
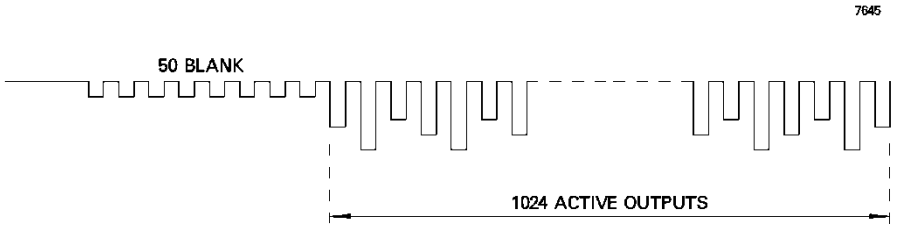


FIGURE 11: LINE OUTPUT FORMAT (Split read-out operation)



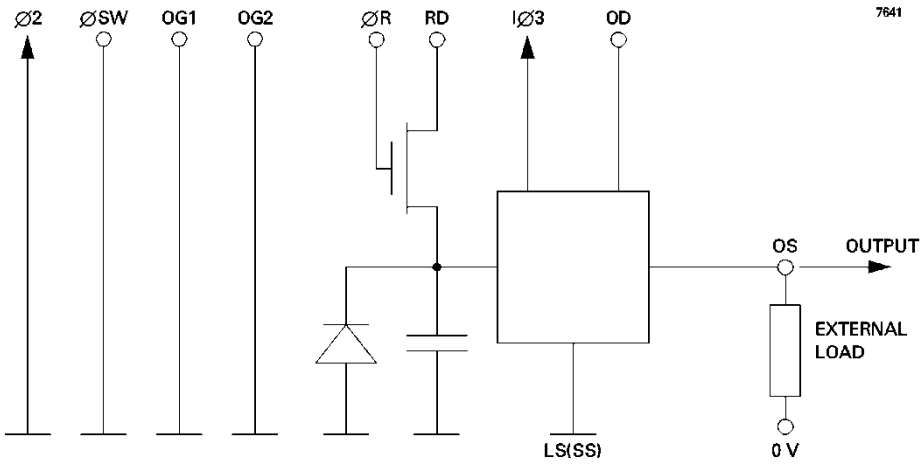
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	Units
T_i	Image clock period	TBA	100 (see note 12)	see note 13	µs
t_{wi}	Image clock pulse width	TBA	50 (see note 12)	see note 13	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	1	5	$0.2T_i$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	t_{ri}	$0.2T_i$	µs
t_{oi}	Image clock pulse overlap	$(t_{ri} + t_{fi})/2$	2	$0.2T_i$	µs
t_{dir}	Delay time, I∅ stop to R∅ start	3	5	see note 13	µs
t_{dri}	Delay time, R∅ stop to I∅ start	1	2	see note 13	µs
T_r	Output register clock cycle period	300	see note 14	see note 13	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ∅R low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

Notes

12. The transfer of a line of charge in back-thinned AIMO devices is affected by a pile-up of the holes used to suppress dark current, as they cannot easily flow to and from the substrate connection when the clocks change state. This problem is eased by extending the t1 timing interval to 50 µs and/or the use of higher drive pulse amplitudes
13. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
14. As set by the readout period.

FIGURE 12: OUTPUT CIRCUIT



Notes

15. The amplifier has a DC restoration circuit which is internally activated whenever I∅3 is high.
16. External load not critical; can be a 3 to 5 mA constant current supply or an appropriate load resistor.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be grounded

Evidence of incorrect handling will invalidate the warranty.

The devices are assembled in a clean room environment and Teledyne e2v recommend that similar precautions are taken by the user to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to ionising radiation. Characterisation data is held at Teledyne e2v with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

TEMPERATURE RANGES

Component	Min	Max
Operating Temperature	-120°C	+75°C
Non-Operating Temperature	-200°C	+100°C
Rate of change		5°C/min

Operation or storage in humid conditions may give rise to ice on the surface when the sensor taken to low ambient temperatures, thereby causing irreversible damage.

GEOMETRY

FIGURE 13: PACKAGE OUTLINE (Tolerances are by design and not verified on each part)