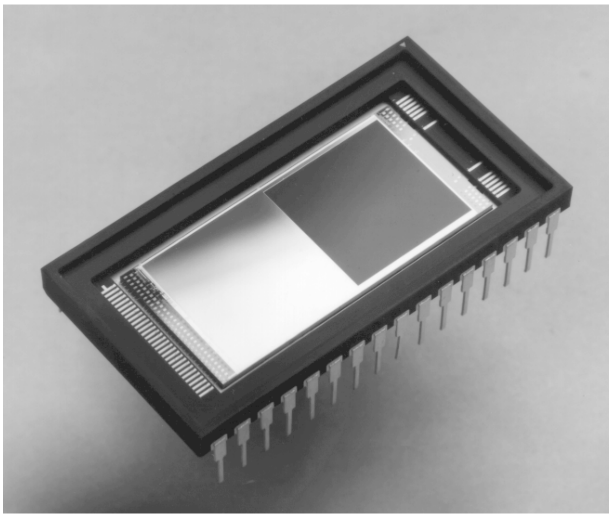
Teledyne e2v

CCD47-20 Back Illuminated NIMO Frame-Transfer High Performance CCD Sensor

FEATURES

- 1024 by 1024 1:1 image format
- Image area 13.3 x13.3 mm
- Back Illuminated format
- Frame transfer operation
- 13 μm square pixels
- Symmetrical anti-static gate protection
- Very low noise output amplifiers
- Gated dump drain on output register
- 100% active area



OVERVIEW

This version of the CCD47 family of CCD sensors has frame transfer architecture. Back illumination technology, in combination with extremely low noise amplifiers, makes the device well suited to the most demanding scientific applications.

This device has a single serial output register. Separate charge detection circuits are incorporated at each end of the register, which is split so that a line of charge can be transferred to either output, or split between the two.

The register is provided with a drain and control gate along the outer edge of the channel for charge dump purposes.

Other variants of the CCD47-20 available are front illuminated format and inverted mode.

Designers are advised to consult Teledyne e2v should they be considering using CCD sensors in abnormal environments or if they require customised packaging.

GENERAL DATA

Format

Image area	13.3 x13.3 mm
Active pixels (H)	1024
(V)	1024
Pixel size	13 x 13 μm
Storage area	13.3 x13.3 mm
Pixels (H)	1024
(V)	1033
Additional pixels are provided in the image area for dark reference and over-scanning purposes.	
Number of output amplifiers	2
Weight (approx, no window)	7.5g

Package

Package size	22.7 x 42.0 mm
Number of pins	32
Inter-pin spacing	2.54 mm
Window material	Removable glass
Package type	Ceramic DIL array

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Approved for public release: Teledyne e2v APPROVED (CM 5002896)

APPLICATIONS

- Spectroscopy
- Scientific Imaging
- Medical Imaging

TYPICAL PERFORMANCE

Maximum readout frequency	5 MHz
Output amplifier responsivity	4.5 μV/e^-
Peak signal	120 ke^-/pixel
Dynamic range (at 20 kHz)	~60,000 : 1
Spectral range	200 – 1100 nm
Readout noise (at 20 kHz)	2 e^- rms

OTHER DATA

PERFORMANCE

Parameter	Min	Typical	Max	Units
Peak charge storage (see note 1)	80k	120k	-	e^-/pixel
Peak output voltage (no binning)	-	540	-	mV
Dark signal at 293 K (see notes 2 and 3)	-	20	40	ke^-/pixel/s
Dynamic range (see note 4)	-	60,000 : 1	-	
Charge transfer efficiency (see note 5):				
parallel	-	99.9999	-	%
serial	-	99.9993	-	%
Output amplifier responsivity (see note 3)	3.0	4.5	6.0	μV/e^-
Readout noise at 253 K (see notes 3 and 6)	-	2.0	4.0	rms e^-/pixel
Maximum readout frequency (see note 7)	-	5.0	-	MHz
Dark signal non-uniformity at 293 K (std. deviation) (see notes 3 and 8)	-	2	4	ke^-/pixel/s

Note: Register capacity is designed to have 4x the image peak charge storage. This is not factory tested.

SPECTRAL RESPONSE AT 243 K

Wavelength (nm)	Minimum Response (QE)						Maximum Response Non-uniformity (1σ)	Units
	Basic Midband Coated	Basic Broadband Coated	Basic Uncoated	Enhanced No Coat	Basic Midband Coated with SAB (B97)	Deep Depletion Enhanced Multi-2 Coated		
350	15	25	10		15	25		%
400	40	55	25		40	75	3	%
500	85	75	55		80	80		%
650	85	75	50		80	80	3	%
900	30	30	30		25	60	5	%

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode Capacitances (Measured at mid-clock level)

	Min	Typical	Max	Units
S∅/S∅ interphase	-	3.5	-	nF
I∅/I∅ interphase	-	3.5	-	nF
I∅/SS and S∅/SS	-	4.5	-	nF
R∅/R∅ interphase	-	40	-	pF
R∅/(SS + DG + OD)	-	60	-	pF
∅R/SS	-	10	-	pF
Output impedance at typical operating conditions	-	300	-	Ω

NOTES

1. Signal level at which resolution begins to degrade. Only factory tested on SAB variants at typical ABD voltage.
2. Measured at 243 K with V_{SS} high, the equivalent at 293 K is then determined from:

   $$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

   where Q_d is the measured darks signal at temperature T and Q_{d0} is the dark signal at 293 K.
3. Test carried out on all sensors.
4. Dynamic range is the ratio of full-well capacity to readout noise measured at 243 K and 20 kHz readout frequency.
5. CCD characterisation measurements made using charge generated by X-ray photons of known energy. Not factory tested.
6. Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 20 µs integration period.
7. Readout at speeds in excess of 5 MHz into a 15 pF load can be achieved but performance to the parameters given cannot be guaranteed. Factory production test are performed at < 50 kHz only.
8. Measured at 243 K and scaled as per note 2. Measurement excludes white defects.

BLEMISH SPECIFICATION

Traps	Pixels where charge is temporarily held. Columns with a trap are counted if they have a capacity greater than 200 e⁻ at 243 K.
Black spots	Are counted when they have a signal level of less than 80% of the local mean at a signal level of approximately half full-well.
White spots	Are counted when they have a generation rate 25 times the specified maximum dark signal generation rate (measured between 243 and 293 K). The typical temperature dependence of white spot blemishes is the same as that of the average dark signal i.e.: $Q_d/Q_{d0} = 122T^3e^{-6400/T}$
White column	A column which contains at least 21 white defects.
Black column	A column which contains at least 21 black defects.

GRADE	0	1	2
Column defects; black or slipped	1	2	6
white	0	0	2
Black spots	50	100	200
Traps >200 e⁻	2	5	12
White spots	50	80	100

Grade 5 Devices which are fully functional, with image quality below that of grade 2, and which may not meet all other performance parameters.

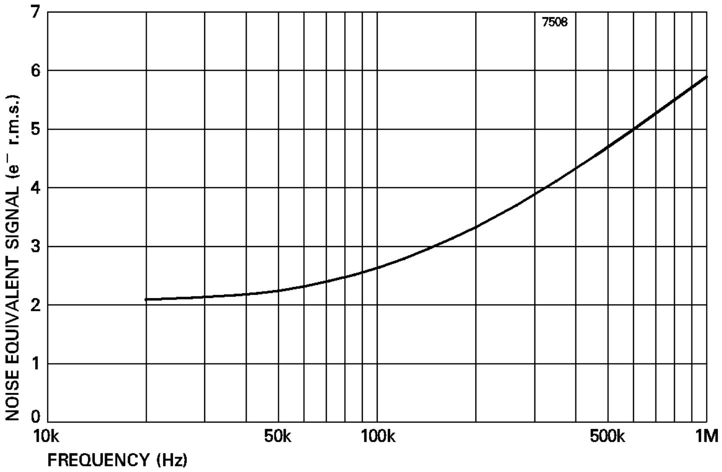
Note: The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 243 K. The amplitude of white spots and columns will decrease rapidly with temperature.

GRAPHS

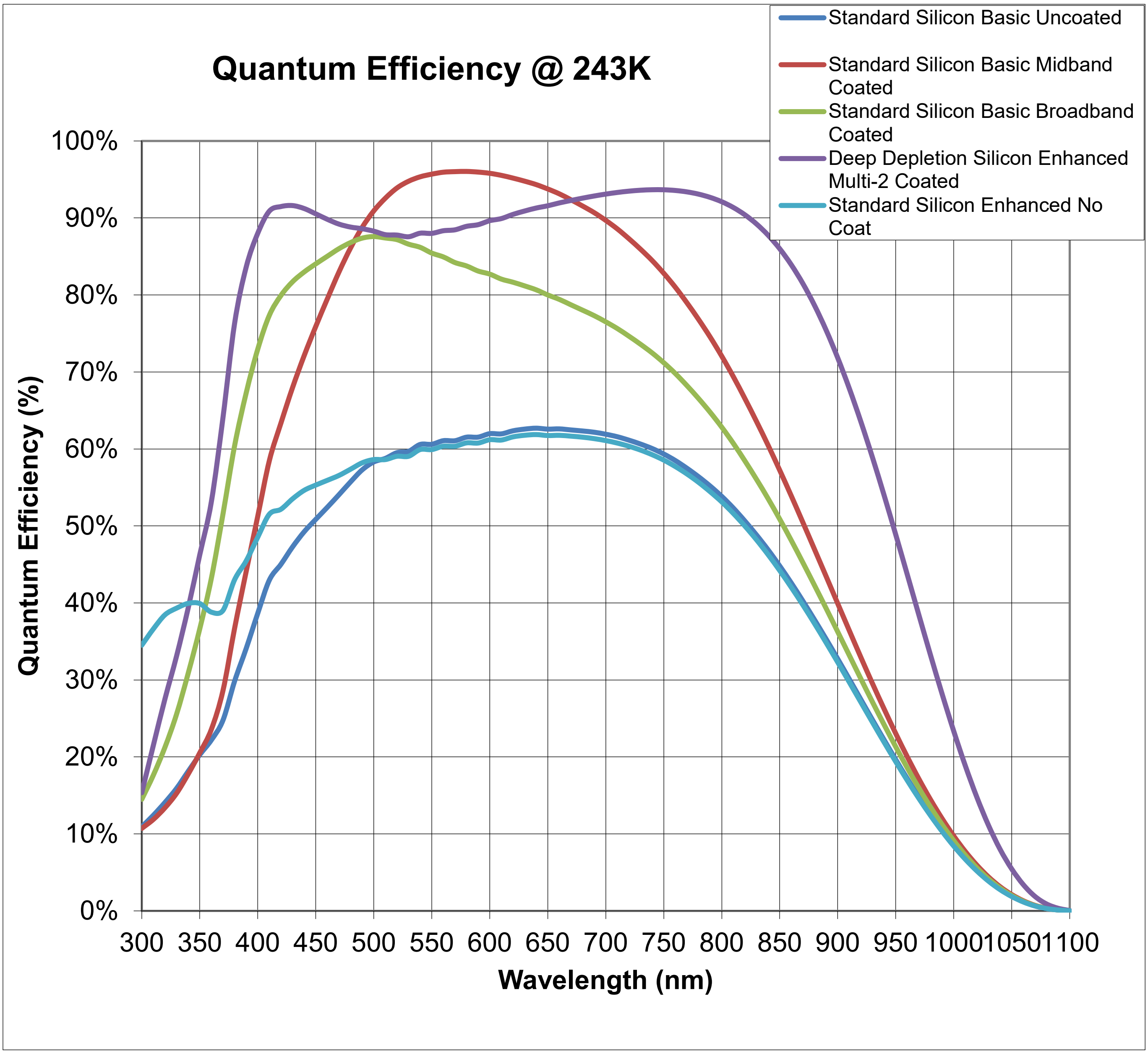
TYPICAL OUTPUT CIRCUIT NOISE

(Measured using clamp and sample)

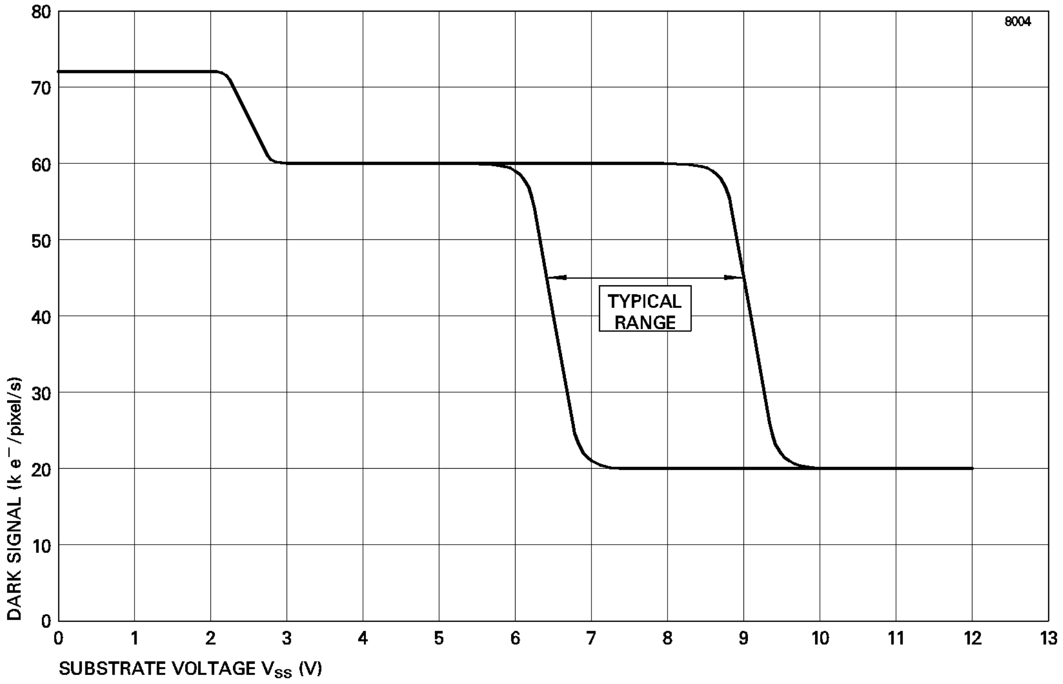
V_{SS} = 9.5 V, V_{RD} = 17 V, V_{OD} = 29 V



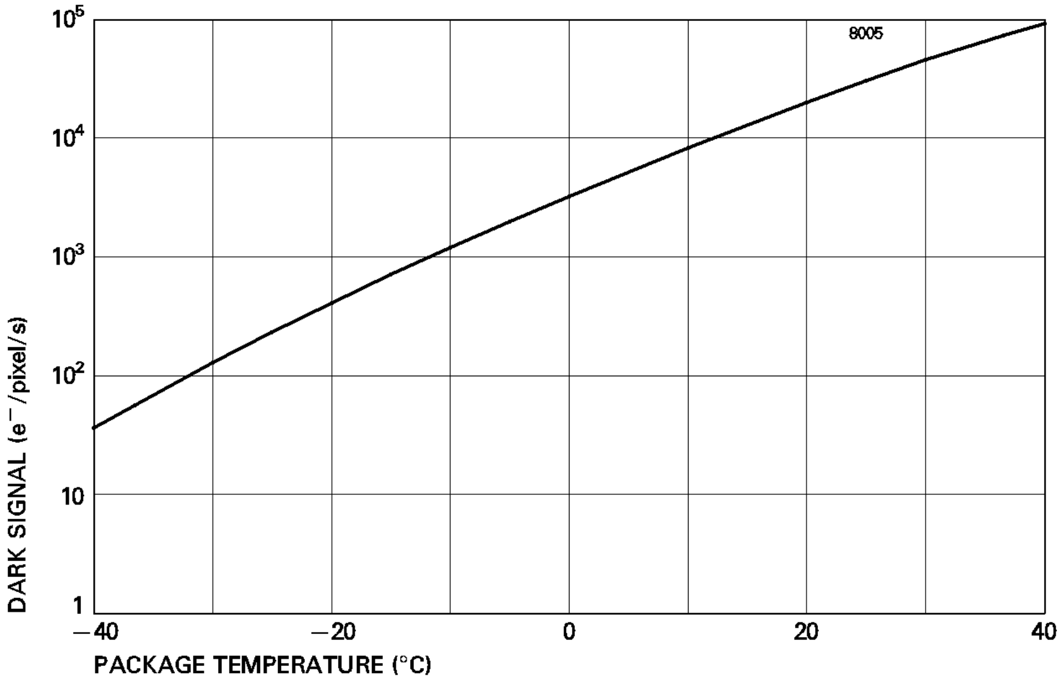
TYPICAL SPECTRAL RESPONSE (At 243K, no window)



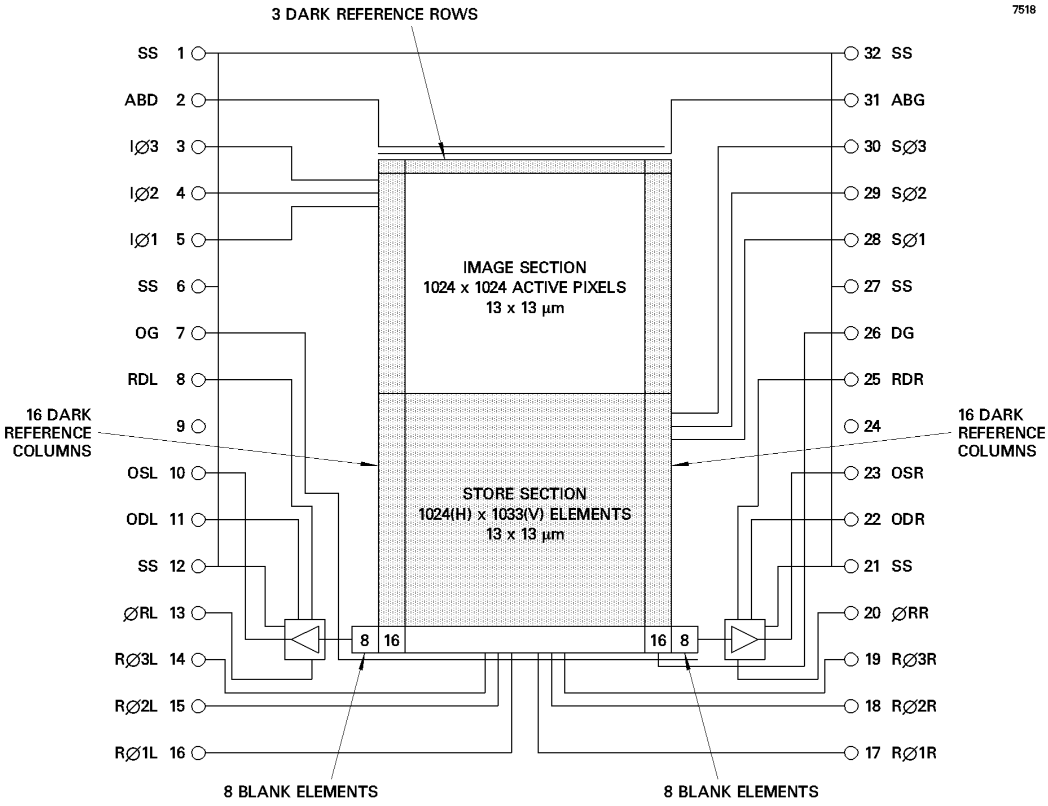
TYPICAL VARIATION OF DARK CURRENT WITH SUBSTRATE VOLTAGE



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE (V_{SS} = +9.5 V)



DEVICE SCHEMATIC



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (See note 9)			MAXIMUM RATINGS with respect to V_{SS}
			Min	Typical	Max	
1	SS	Substrate	0	9	10	-
2	ABD	Anti-blooming drain (see note 10)	17	20	24	–0.3 to +25 V
3	I∅3	Image area clock, phase 3	8	12	15	±20 V
4	I∅2	Image area clock, phase 2	8	12	15	±20 V
5	I∅1	Image area clock, phase 1	8	12	15	±20 V
6	SS	Substrate	0	9	10	-
7	OG	Output gate	1	3	5	±20 V
8	RDL	Reset transistor drain (left amplifier)	15	17	19	–0.3 to +25 V
9	-	No connection		-		-
10	OSL	Output transistor source (left amplifier)		see note 11		–0.3 to +25 V
11	ODL	Output transistor drain (left amplifier)	27	29	32	–0.3 to +35 V
12	SS	Substrate	0	9	10	-
13	∅RL	Output reset pulse (left amplifier)	8	12	15	±20 V
14	R∅3L	Output register clock phase 3 (left section)	8	10	15	±20 V
15	R∅2L	Output register clock phase 2 (left section)	8	10	15	±20 V
16	R∅1L	Output register clock phase 1 (left section)	8	10	15	±20 V
17	R∅1R	Output register clock phase 1 (right section)	8	10	15	±20 V
18	R∅2R	Output register clock phase 2 (right section)	8	10	15	±20 V
19	R∅3R	Output register clock phase 3 (right section)	8	10	15	±20 V
20	∅RR	Output reset pulse (right amplifier)	8	12	15	±20 V
21	SS	Substrate	0	9	10	-
22	ODR	Output transistor drain (right amplifier)	27	29	32	–0.3 to +35 V
23	OSR	Output transistor source (right amplifier)		see note 11		–0.3 to +25 V
24	-	No connection		-		-
25	RDR	Reset transistor drain (right amplifier)	15	17	19	–0.3 to +25 V
26	DG	Dump gate (see note 12)	-	0	-	±20 V
27	SS	Substrate	0	9	10	-
28	S∅1	Storage area clock, phase 1	8	12	15	±20 V
29	S∅2	Storage area clock, phase 2	8	12	15	±20 V
30	S∅3	Storage area clock, phase 3	8	12	15	±20 V
31	ABG	Anti-blooming gate	0	0	5	±20 V
32	SS	Substrate	0	9	10	-

Maximum voltages between pairs of pins:
pin 10 (OSL) to pin 11 (ODL)............... +15 V
pin 22 (ODR) to pin 23 (OSR) .... +15 V
Maximum output transistor current...........10 mA

NOTES

9. Readout register clock pulse low levels +1 V; other clock low levels 0 ± 0.5 V.

10. Voltage min and max values given are for SAB variants. Modulation of ABD will adjust the pixel capacity, with increasing capacity for lower values of ABD. There is natural variation device to device on the exact capacity provided by a given ABD. For non-SAB variants, the pixel drain is not incorporated, but bias is still necessary to avoid spurious charge injection. The same voltage limits can be used, or alternatively ABD can be tied to OD to reduce the number of voltage supplies if operating with substrate high, but the maximum rating with respect to Vss should be observed during the power on and off sequence, i.e. raise drains to mid-level, raise SS then raise drains to values shown. Performance for non-SAB variants is insensitive to the ABD bias in the range given.

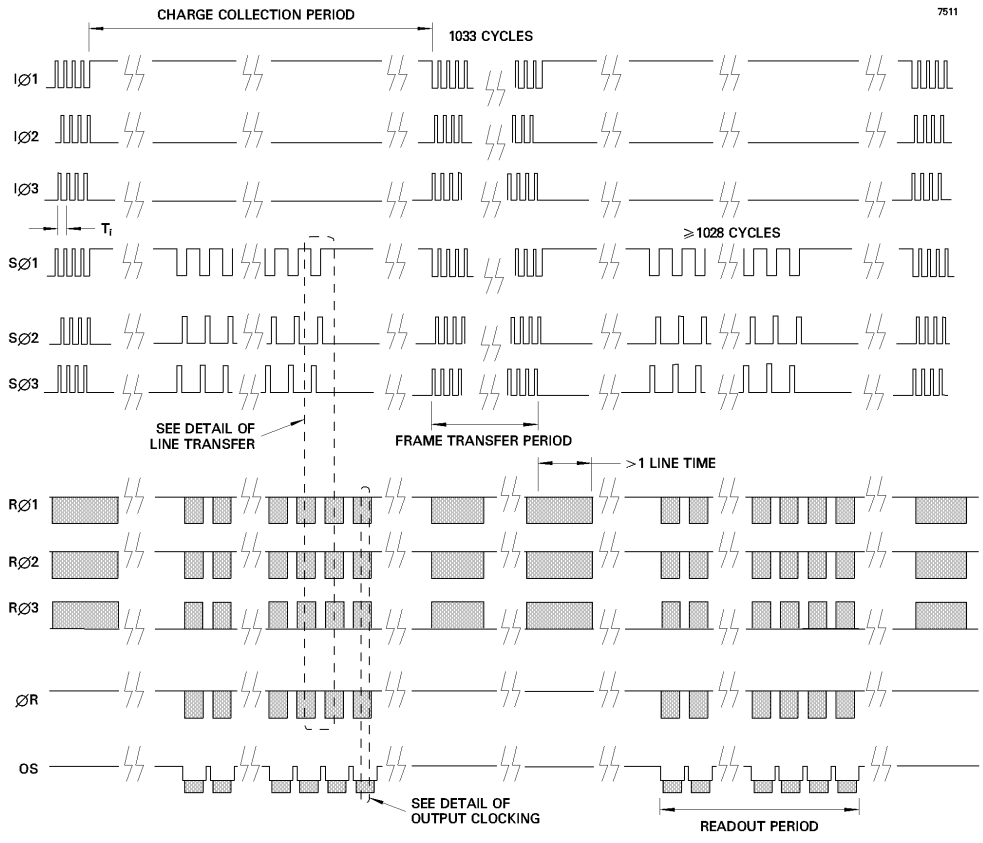
11. 3 to 5 V below OD. Connect to ground using a 2 to 5 mA current source or appropriate load resistor (typically 5 to 10 kΩ).

12. Non-charge dumping level shown. For operation in charge dumping mode, DG should be pulsed to 12 ± 2 V.

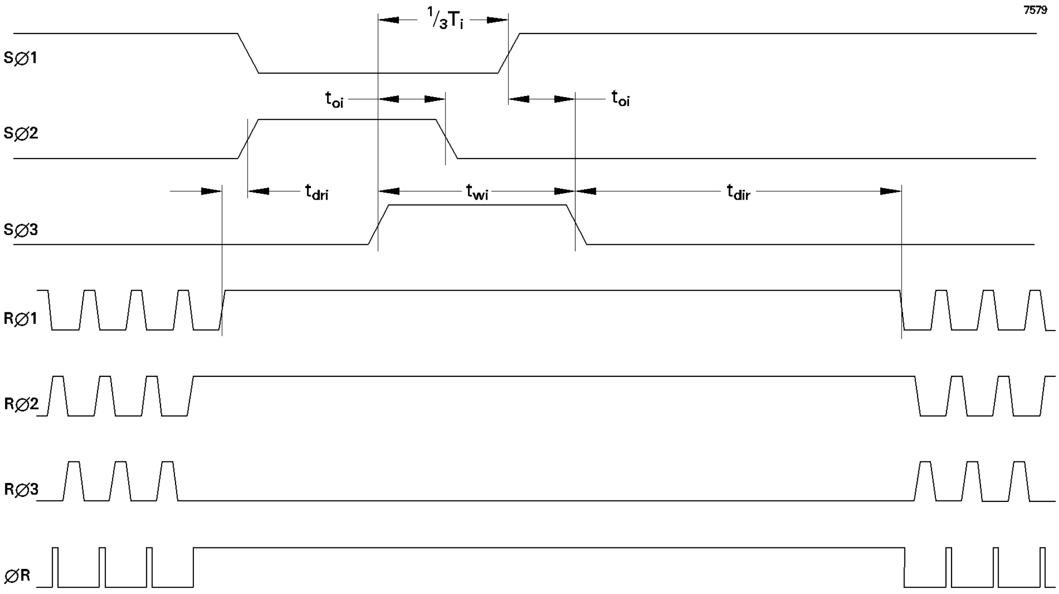
13. All devices will operate at the typical values given. However, some adjustment within the minimum to maximum range may be required to optimise performance for critical applications. It should be noted that conditions for optimum performance may differ from device to device.

14. With the R∅ connections shown, the device will operate through the right-hand output only. In order to operate from both outputs, R∅1(L) and R∅2(L) should be reversed.

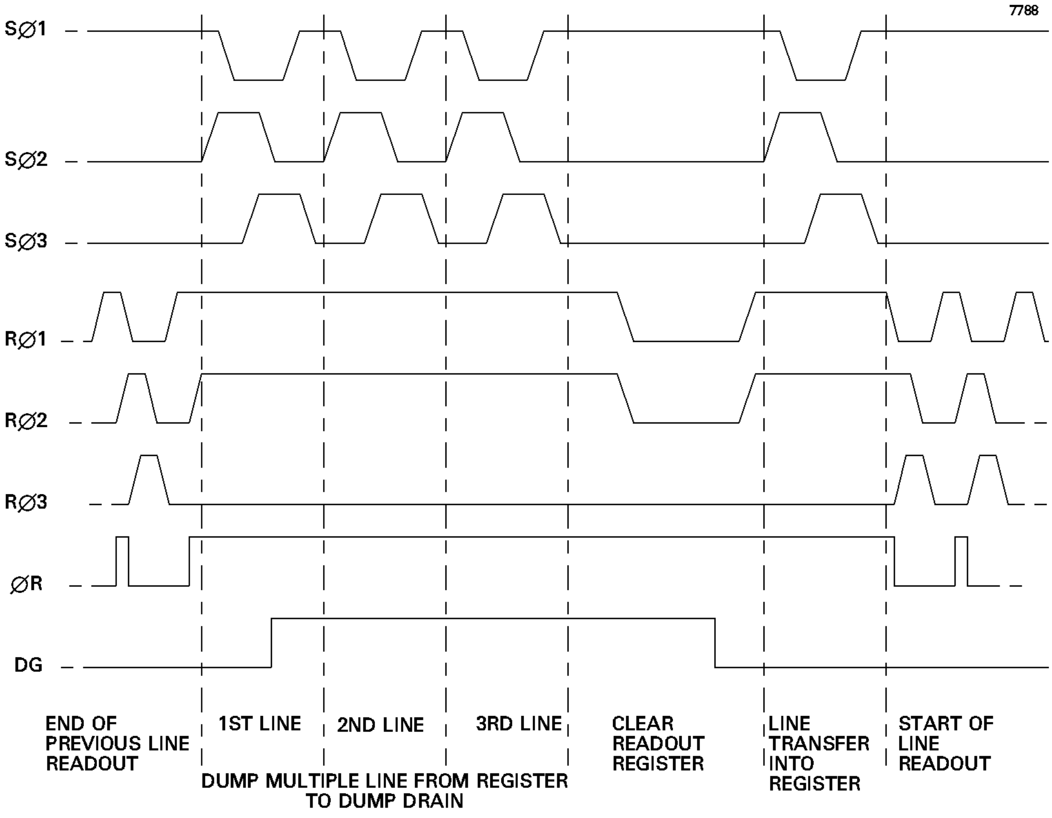
FRAME TRANSFER TIMING DIAGRAM



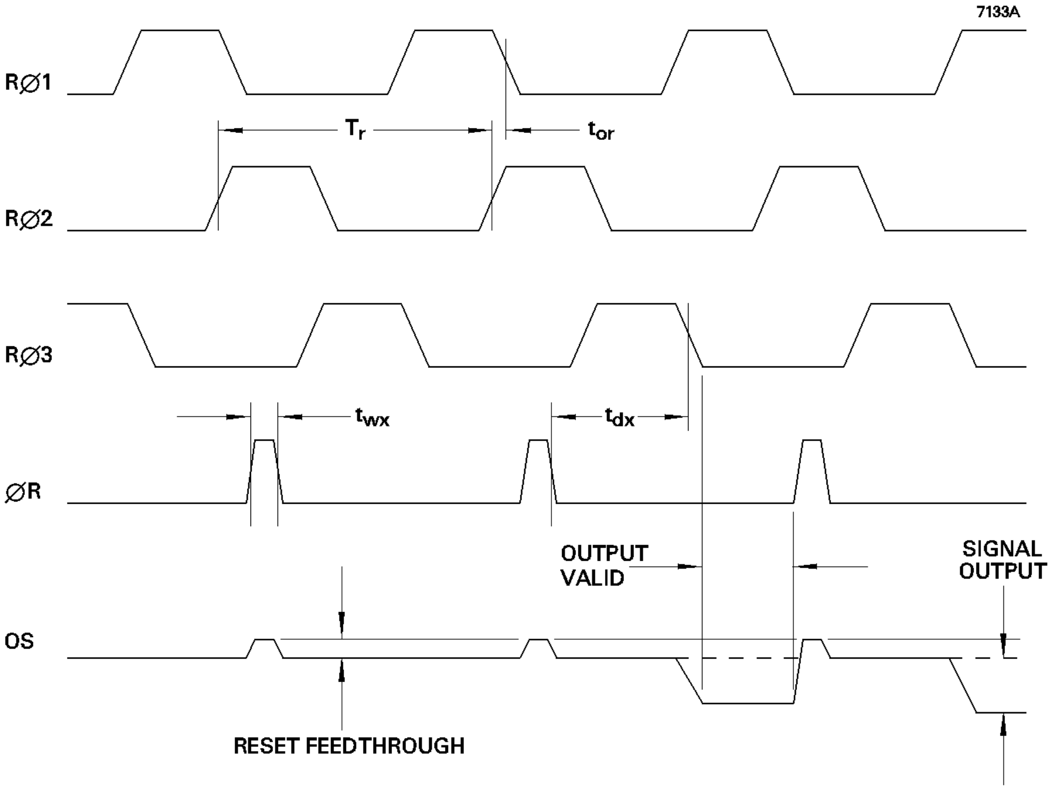
DETAIL OF LINE TRANSFER



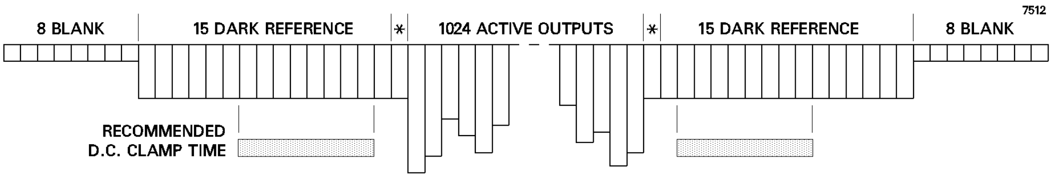
DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



* = Partially shielded transition elements

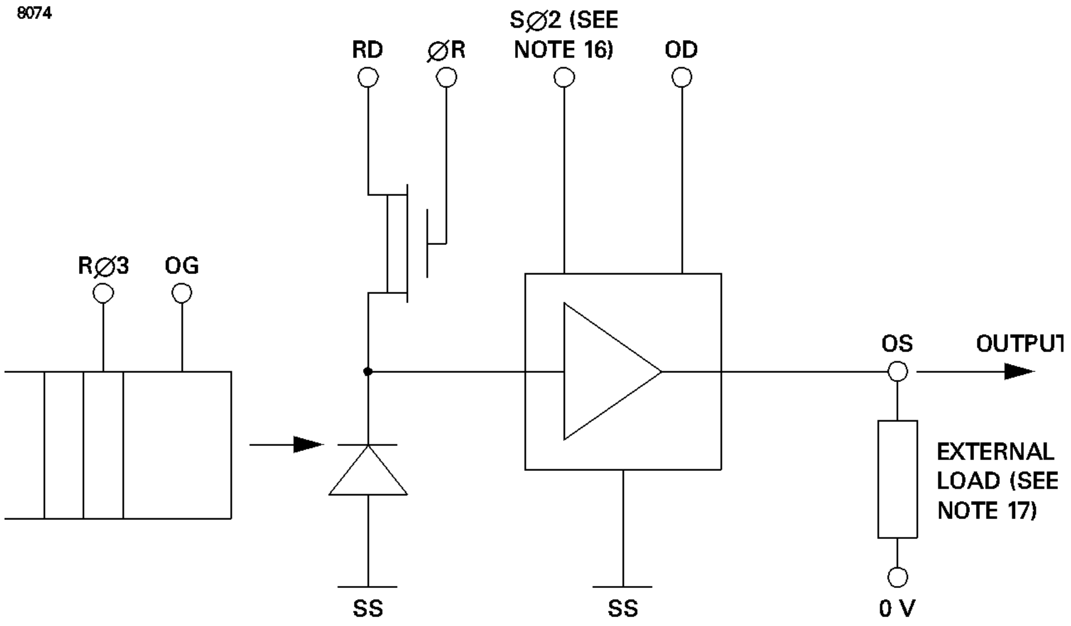
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	Units
T_i	Store clock period	2	5	see note 15	µs
t_{wi}	Image/store clock pulse width	1	2.5	see note 15	µs
t_{ri}	Image/store clock pulse rise time (10 to 90%)	0.1	0.5	$0.2T_i$	µs
t_{fi}	Image/store clock pulse fall time (10 to 90%)	t_{ri}	0.5	$0.2T_i$	µs
t_{oi}	Image/store clock pulse overlap	$(t_{ri} + t_{fi})/2$	0.5	$0.2T_i$	µs
t_{dir}	Delay time, S∅ stop to R∅ start	1	1	see note 15	µs
t_{dri}	Delay time, R∅ stop to S∅ start	1	1	see note 15	µs
T_r	Output register clock cycle period	200	1000	see note 15	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	$0.2t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ∅R low to R∅3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

15.No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.

OUTPUT CIRCUIT



NOTES

16.The amplifier has a DC restoration circuit which is internally activated whenever S∅2 is high.

17.Not critical; can be a 3 to 5 mA constant current supply or an appropriate load resistor.

HEALTH AND SAFETY HAZARDS

Teledyne e2v devices are safe to handle and operate, provided that the relevant precautions stated herein are observed. Teledyne e2v does not accept responsibility for damage or injury resulting from the use of devices it produces. Equipment manufacturers and users must ensure that adequate precautions are taken. Appropriate warning labels and notices must be provided on equipment incorporating Teledyne e2v devices and in operating manuals.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All gate electrodes are provided with internal protections circuits but not the other pins.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising radiation.

Users planning to use CCDs in a high radiation environment are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	**Typical**	**Max**	
Non-operating	153	293	353	K
Operating	153	273	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

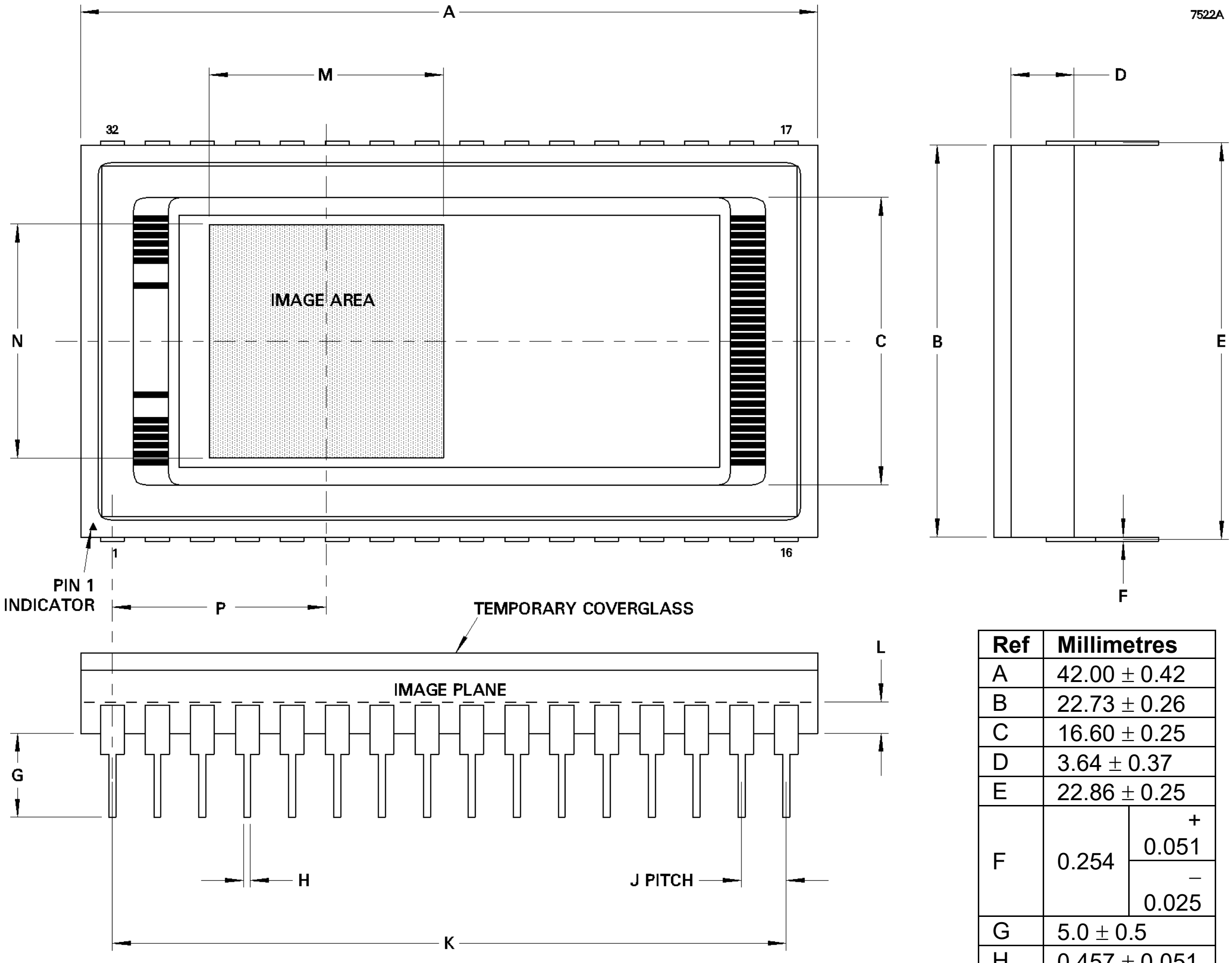
Maximum device heating/cooling ....5 K/min

High Voltage

X-Ray Radiation

OUTLINE DRAWINGS

All dimensions shown in mm. Dimensions without limits are nominal.



Ref	Millimetres
A	42.00 ± 0.42
B	22.73 ± 0.26
C	16.60 ± 0.25
D	3.64 ± 0.37
E	22.86 ± 0.25
F	0.254 $^{+0.051}_{-0.025}$
G	5.0 ± 0.5
H	0.457 ± 0.051
J	2.54 ± 0.13
K	38.1
L	1.65 ± 0.25
M	13.3
N	13.3
P	12.2 ± 0.5