CCD55-30 AIMO Back Illuminated High Performance CCD Sensor

INTRODUCTION

The CCD55-30 is one of the CCD55 range of large area image sensors primarily intended to suit the requirements of astronomy, medical diagnostic and scientific measuring instruments. The device utilises Advanced Inverted-Mode Operation (AIMO) for lowest dark current. It operates with standard three-phase clocking and buried channel charge transfer. The read-out register has a low-noise amplifier at one end for slow-scan applications and a high speed amplifier at the other end.

DESCRIPTION

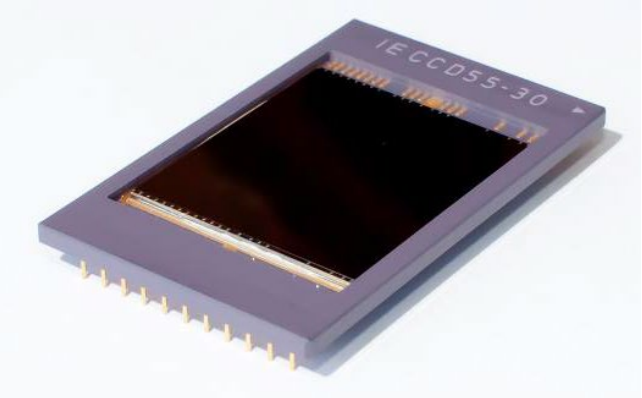
The sensor has an image area with 1252 x 1152 pixels for Full Frame variants. Frame Transfer variants can also be produced by application of a metal “store shield” leaving an unobstructed image area of 1242 x 574 usable pixels. There is a single output register that has charge detection circuits incorporated at each end. One output (A1) is intended for high-speed operation and has an associated dummy output circuit. By design the maximum speed of this output is approximately 6 MHz, as set by being sufficiently settled for reliable CDS with ≤10 pF load, but operation up to 9 MHz should be achievable if incomplete settling can be tolerated. This output is designed to have charge handling capacity of at least two image pixels. The second output (A2) is designed for lower noise performance whilst still being able to handle the full well capacity of one pixel and by design has a maximum speed of approximately 3 MHz.

VARIANTS

Multiple AR coatings are available as well as the choice between Full Frame and Frame Transfer variants. Attachment of permanent windows is also an option and should be discussed directly with Teledyne e2v.

Non-inverted-mode options (NIMO) and other formats (e.g. CCD55-20) can also be provided and are described in other data sheets.

Consult Teledyne e2v technologies for any further information.



The device pictured is without a store shield.

SUMMARY SPECIFICATION

Total number of pixels		1252 (H) x 1152 (V)
Number of usable image pixels in Frame Transfer variant		1242 (H) x 574 (V)
Pixel size		22.5 µm square
Total pixel area		28.2 mm x 25.9 mm
Outputs		2
Package size		53.34 mm x 33.02 mm
Package format		Ceramic 44-pin
Connectors		Dual-In-Line (DIL)
Amplifier responsivity	A1	1.0 µV/e^-
	A2	2.7 µV/e^-
Read-out noise	A1	6.5 e^- at 18.5 kHz 15 e^- at 1 MHz (estimate)
Read-out noise	A2	3.5 e^- at 18.5 kHz 8 e^- at 1 MHz (estimate)
Maximum data rate A1		6 MHz
Image pixel capacity		400,000 e^-
Dark signal (at 0 °C)		90 e^-/pixel/second

Quoted performance parameters given here are “typical” values. Specification limits are shown later.

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PERFORMANCE

Electro-Optical Specification

Note 1		Min	Typical	Max	Units	Note
Peak charge storage (image)			400,000		e^-/pixel	2,3
Peak charge storage (register)			1,300,000		e^-/pixel	2,3
Output node capacity	A1		1,300,000		e^-	2,3
	A2		600,000		e^-	
Output amplifier responsivity	A1	0.8	1.0	1.6	µV/e^-	
	A2	2	2.7	4	µV/e^-	
Read-out noise	A1		6.5		e^- rms	4
	A2		3.5	5	e^- rms	
Dark signal	at 273 K		70	110	e^-/pixel/s	5
	at 293 K		800	1300	e^-/pixel/s	
Dark Signal Non-Uniformity	at 273 K		30	53	e^-/pixel/s	5
	at 293 K		185	325	e^-/pixel/s	
Charge transfer efficiency	serial		99.9999		%	2,6
	parallel		99.9993		%	

NOTES

1. Device performance will be within the limits specified by “max” and “min” when operated at the recommended voltages supplied with the test data and when measured at a typical register clock frequency of 50 kHz. Performance at higher readout frequencies is not measured for production testing at Teledyne e2v. The readout frequency for noise is defined separately in note 4.
2. Typical values are provided from results of previous measurement or by design and by default are not measured per device.
3. Signal level at which resolution begins to degrade.
4. Measured at 253 K with an 18.5 kHz readout frequency.
5. Dark signal (or current) is measured with the substrate voltage at +9V and the device temperature 273 K. It is a strong function of temperature and the typical AIMO average dark current Q_d any temperature T (Kelvin) between 230 K and 300 K is given by:

   $Q_d/Q_{do} = 1.14x10^6T^3e^{-9080/T}$

   where Q_{do} is the dark current at 293 K.

   The dark signal and DSNU will be reported at 293K only.

   Note, DSNU scales with temperature generally following the NIMO scaling of $Q_d/Q_{do} = 122T^3e^{-6400/T}$.

   Transfer through the image sections can give rise to an additional temperature-independent signal component called “clock-induced charge” The CIC generated depends on the bias levels used, whether the device operates in inverted or non-inverted mode, and the details of the clock timings employed. Further details can be found on the Teledyne e2v website or by contacting Teledyne e2v.
6. The CTE value is quoted for the complete clock cycle (i.e. all phases).

COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

Grade		0	1	2
Column defects	Black	0	2	6
	White	0	0	2
White spots		80	100	150
Black spots		50	100	400
Traps > 200e^-		2	5	12

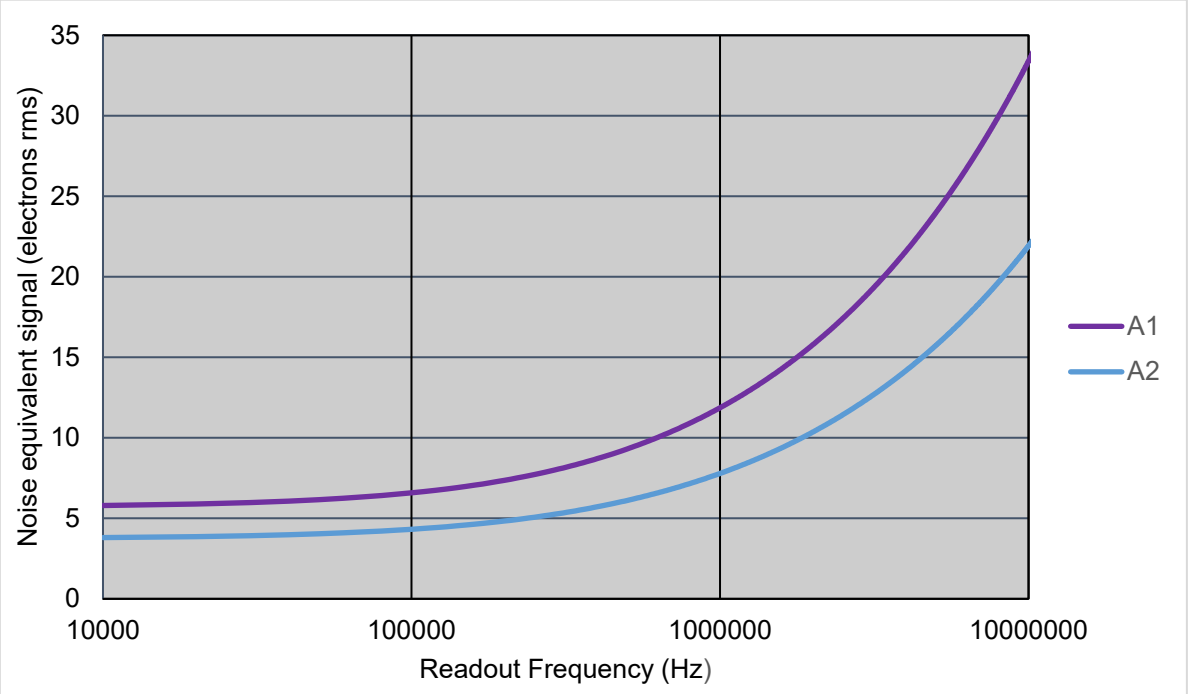
Grade 5 devices are fully functional but with an image quality below that of grade 2, and may not meet all other specifications. Not all parameters may be tested.

DEFINITIONS

White spots	A defect is counted as a white spot if the dark generation rate is 50 times the specified maximum dark signal generation rate at 293 K. The typical temperature dependence of white spot defects is different from the average dark signal and is given by: $Q_d/Q_{do} = 122T^3e^{-6400/T}$
Black spots	A black spot defect is a pixel with less than 80% of the local mean at a signal level of approximately half full well.
Column defects	A column is counted as a defect if it contains at least 9 white or dark single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel. Columns containing these are counted as trap defects if the quantity of trapped charge is greater than 200 e^- at the specified test temperature (nominally 273 K).

TYPICAL OUTPUT AMPLIFIER NOISE

The theoretical variation of typical read noise with operating frequency is shown below, if measured using correlated double sampling with a pre-sampling bandwidth equal to twice the pixel rate at approximately 253 K.



SPECTRAL RESPONSE AT 253 K (–20 ˚C)

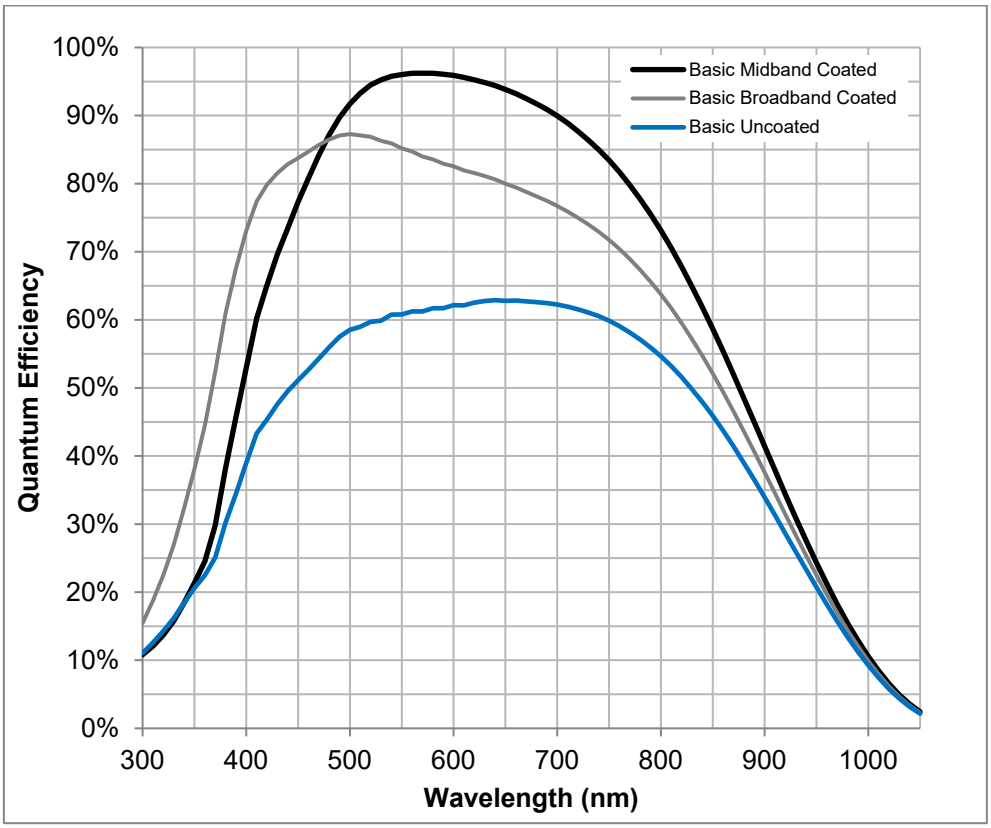
Wavelength (nm)	Minimum QE (%)			Maximum Pixel Response Non-Uniformity PRNU (1σ) (%)
	Basic Process Mid Band Coated	Basic Process Broad Band Coated	Basic Process Uncoated [7]	
350	15	25	10	-
400	40	55	25	3
500	85	75	55	-
650	85	75	50	3
900	25	25	25	5

NOTE

7. Only available in Full Frame format.

TYPICAL QE VALUES FROM MODEL CALCULATION

Model inputs: Basic back thinning process, temperature -20 °C, silicon thickness 16.00 µm, typical AR coating layer thickness, incoherent reflection.



NOTES

8 Manufacturing process variation can mean actual sensor QE performance may differ from the typical values in these curves, but will meet minimum QE values from the spectral response table above. QE measurements are averaged over many pixels and over the pass band of the optical filter.

9 The values here represent performance at -20 °C. QE at longer wavelengths will decrease at much lower temperatures and increase when temperature rises. Contact Teledyne e2v for more information.

DEFINITIONS

Back-Thinning

A back-thinned CCD is fabricated on the front surface of the silicon and is subsequently processed for illumination from the reverse side. This avoids loss of transmission in the electrode layer (particularly significant at shorter wavelengths or with low energy X-rays). This process requires the silicon to be reduced to a thin layer by a combination of chemical and mechanical means. The surface is “passivated” and an anti-reflection coating may be added.

AR Coating

Anti-reflection coatings are normally applied to the back illuminated CCD to further improve the quantum efficiency. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For X-ray detection, an uncoated device may be preferable.

Advanced Inverted Mode Operation (IMO)

An inverted mode (IMO) CCD has an additional implant that allows charge integration to be carried out with all clock phases low. With a high voltage applied to the substrate (typically +9 V) this causes the whole of the device to be flooded with holes (inverted or pinned), which suppresses the surface component of dark signal. This leaves only the much lower bulk component, reducing the overall dark signal by a factor of approximately 100.

An Advanced Inverted Mode Operation (AIMO) CCD is a structure developed by Teledyne e2v to achieve higher peak signal levels. This mode of operation does not allow reverse clocking of charge in the image area.

Readout Noise

Readout noise is the random noise from the CCD output stage in the absence of signal. This noise introduces a random fluctuation in the output voltage that is superimposed on the detected signal.

The method of measurement involves reverse-clocking the register and determining the standard deviation of the output fluctuations, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dummy Output

Output A1 has an associated “dummy” circuit on-chip, which is of identical design to the “real” circuit but receives no signal charge. The dummy output should have the same levels of clock feed-through, and can thus be used to suppress the similar component in the “real” signal output by means of a differential pre-amplifier. The penalty is that the noise is increased by a factor of $\sqrt{2}$. As the dummy output uses the same OD as the “real” output, it can’t be powered down but does not need to be used for common mode noise rejection if this is not required.

Dark Signal

This is the output signal of the device with zero illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration. Dark signal is a strong function of temperature as described in note 5.

Correlated Double Sampling

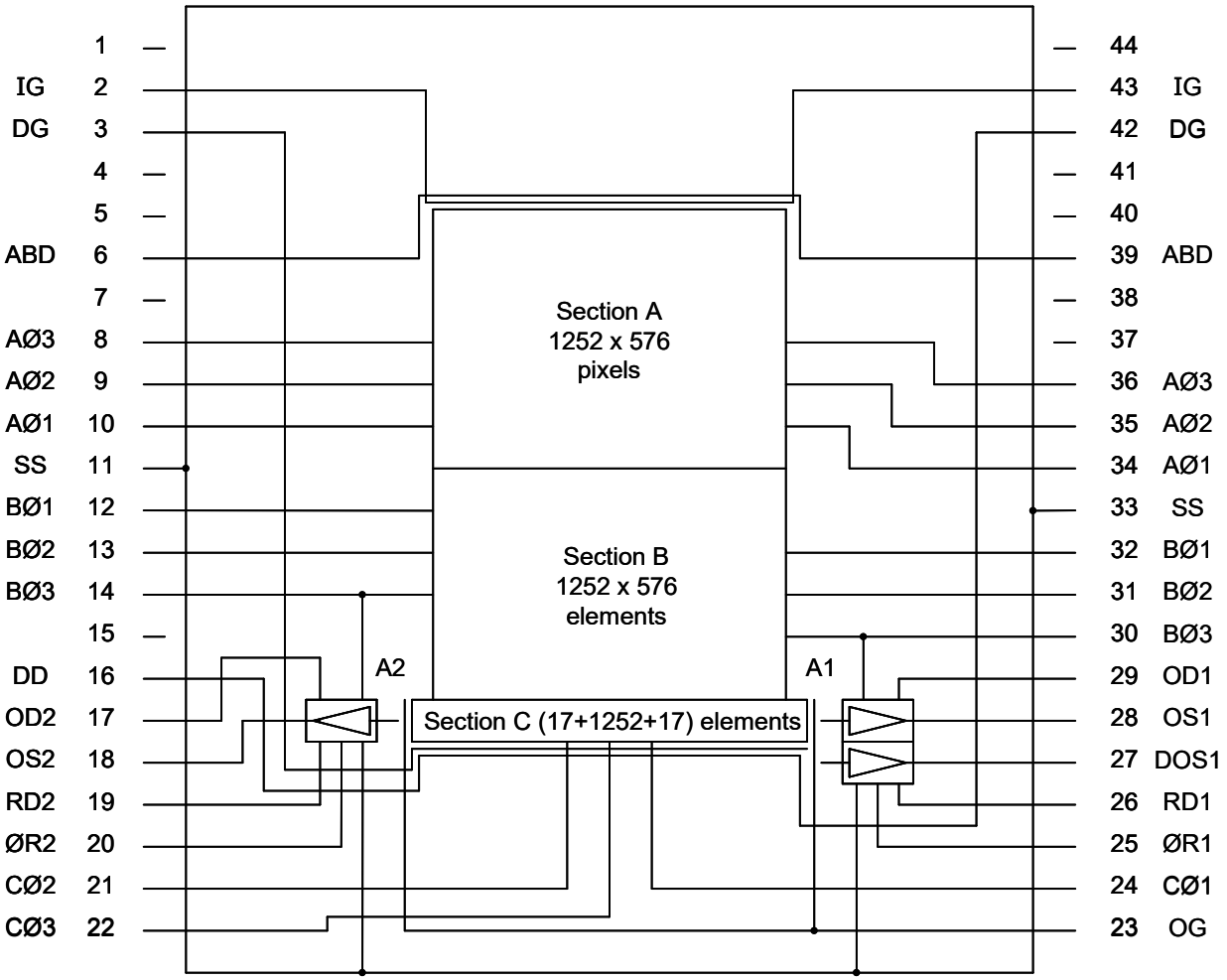
A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

Charge Transfer Efficiency

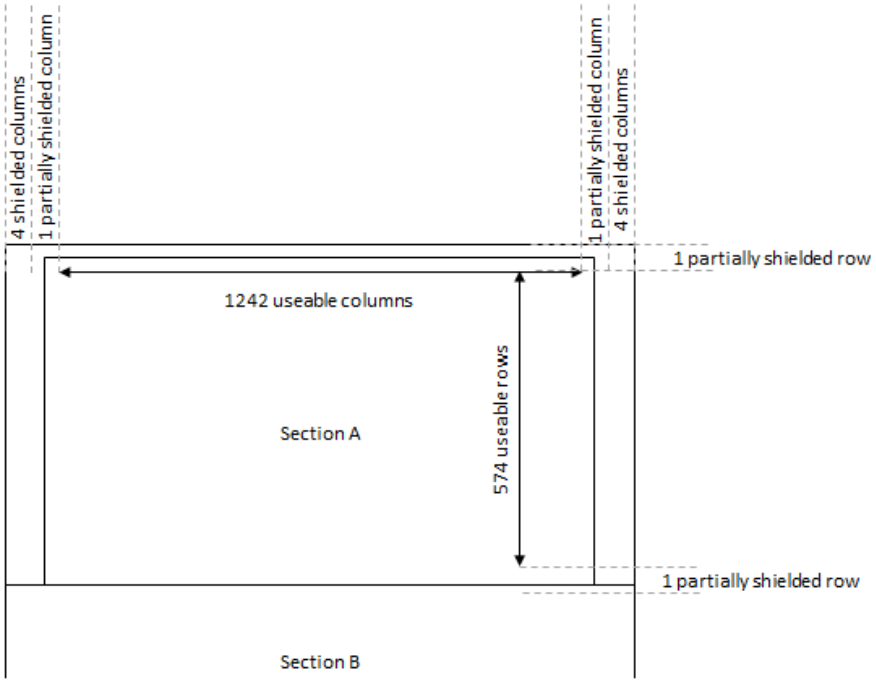
The fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature and clock frequency.

ARCHITECTURE

Device Schematic

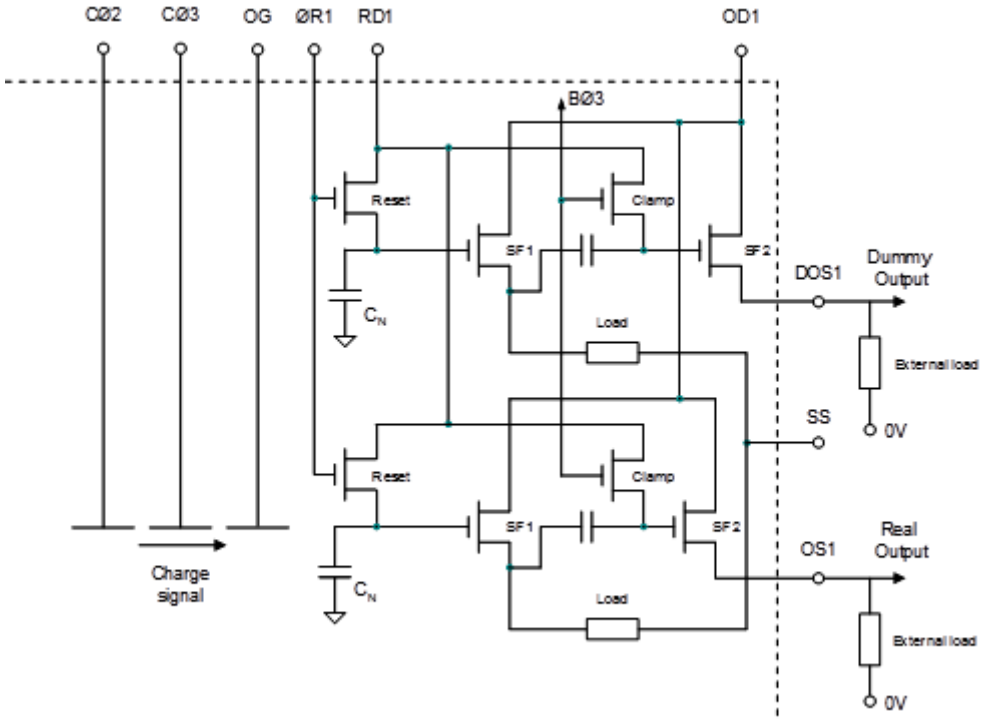


Frame Transfer Image Area

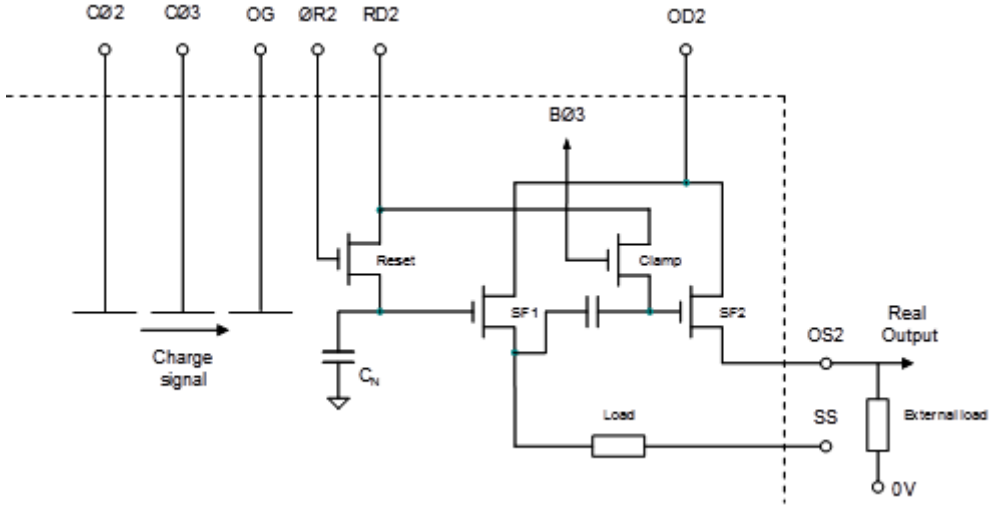


OUTPUT CIRCUITS

Large Signal (A1)



Low Noise (A2)



NOTES

10. The DC restoration circuitry requires a pulse at the start of line read-out, and this is automatically obtained by an internal connection to the BØ3 image clock, as can be seen in the schematics.
11. The external load on the large signal output is not critical, but can be 7.5 mA constant current supply or a 3.3 kΩ resistor. The amplifier output impedance is typically 250 Ω for A1.
12. The external load on the low noise output is not critical, but can be 5 mA constant current supply or a 5 kΩ resistor. The amplifier output impedance is typically 400 Ω for A2.

ELECTRICAL INTERFACE

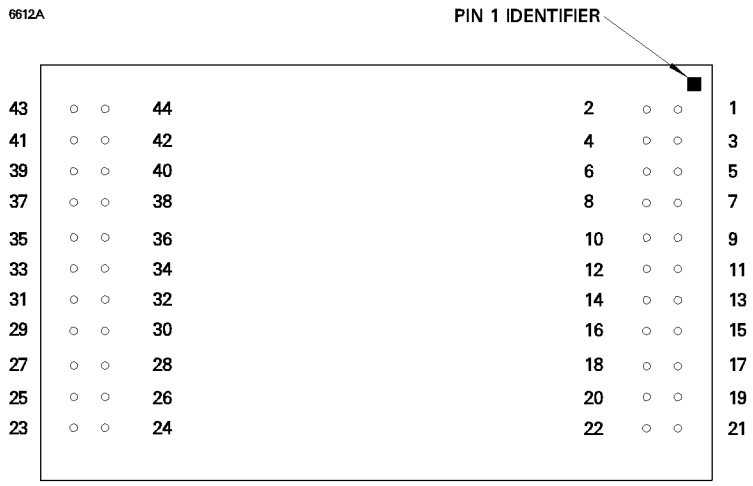
CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 13)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	-	No connection		-		-
2	IG	Isolation gate	-5	0	1	±20V
3	DG	Dump gate (see note 14)	-5	0	1	±20V
4	-	No connection		-		-
5	-	No connection		-		-
6	ABD	Anti-blooming drain (see note 15)	20	22	25	-0.3 to +25V
7	-	No connection		-		-
8	AØ3	Section A drive pulse phase 3	10	12	15	±20V
9	AØ2	Section A drive pulse phase 2	10	12	15	±20V
10	AØ1	Section A drive pulse phase 1	10	12	15	±20V
11	SS	Substrate (see note 16)	8	9	11	-
12	BØ1	Section B drive pulse phase 1	10	12	15	±20V
13	BØ2	Section B drive pulse phase 2	10	12	15	±20V
14	BØ3	Section B drive pulse phase 3	10	12	15	±20V
15	-	No connection		-		-
16	DD	Dump Drain	20	22	25	-0.3 to +25V
17	OD2	A2 Output drain (see note 17)	27	30	32	-0.3 to +34V
18	OS2	A2 Output transistor source	(see notes 12 and 18)			-0.3 to +34V
19	RD2	A2 Reset transistor drain	15	18	19	-0.3 to +25V
20	ØR2	A2 Output reset pulse	8	12	15	±20V
21	CØ2	C section drive pulse (see note 19)	10	12	15	±20V
22	CØ3	C section drive pulse phase 3	10	12	15	±20V
23	OG	Output Gate, A1 and A2	2	3	5	±20V
24	CØ1	C section drive pulse (see note 20)	10	12	15	±20V
25	ØR1	A1 Output reset pulse	8	12	15	±20V
26	RD1	A1 Reset transistor drain	15	18	19	-0.3 to +25V
27	DOS1	A1 Dummy output source	(see notes 11 and 21)			-0.3 to +34V
28	OS1	A1 Output transistor source	(see notes 11 and 21)			-0.3 to +34V
29	OD1	A1 Output drains (see note 17)	27	30	32	-0.3 to +34V
30	BØ3	Section B drive pulse phase 3	10	12	15	±20V
31	BØ2	Section B drive pulse phase 2	10	12	15	±20V
32	BØ1	Section B drive pulse phase 1	10	12	15	±20V
33	SS	Substrate (see note 16)	8	9	11	-
34	AØ1	Section A drive pulse phase 1	10	12	15	±20V
35	AØ2	Section A drive pulse phase 2	10	12	15	±20V
36	AØ3	Section A drive pulse phase 3	10	12	15	±20V
37	-	No connection		-		
38	-	No connection		-		
39	ABD	Anti-blooming drain (see note 15)	20	22	25	-0.3 to +25V
40	-	No connection	-	-		
41		No connection				
42	DG	Dump Gate (see note 14)	-5	0	1	±20V
43	IG	Isolation Gate (see note 13)	-5	0	1	±20V
44		No connection				

NOTES

13. Reset and the A and B section clock pulse low levels should be 0 ± 0.5 V. The C section clock pulse low level should be set 1 V higher.
14. Non-charge dumping level shown. For charge dumping, DG should be 13 ± 1 V for 12 V register clocks.
15. The device has no anti-blooming but a drain bus is present above section A and must be biased to prevent charge injection. The isolation gate IG is positioned between this bus and the first AØ1 electrode.
16. The substrate voltage may need to be adjusted within the range indicated to achieve correct inverted mode operation.
17. Various guard diodes are connected to the output drains and bias must be maintained. It is not therefore possible to switch off an unused amplifier.
18. Do not connect to voltage supply but use an external load, note 8. With a 5 mA constant-current load, VOS ~ VRD + 6 V. The current through this pin must not exceed 20 mA. Permanent damage may result if, in operation, OS experiences short circuit conditions.
19. Phase 2 for read-out through amplifier A2, phase 1 for read-out through amplifier A1.
20. Phase 1 for read-out through amplifier A2, phase 2 for read-out through amplifier A1.
21. Do not connect to voltage supply but use an external load, note 9. With a 7.5 mA constant-current load, VOS ~ VRD + 6V. The current through this pin must not exceed 20 mA. Permanent damage may result if, in operation, OS or DOS experience short circuit conditions.

PIN CONNECTIONS (View facing underside of package)



ELECTRICAL INTERFACE CHARACTERISTICS

Electrode Capacitances (calculated at mid-clock level)

	Typical	Units
AØ or BØ inter-phase	2.8	nF
AØ1 or BØ1 to SS	21	nF
AØ2, AØ3, BØ2 and BØ3, each to SS	8.4	nF
CØ inter-phase	110	pF
CØ/(SS + DG +DD)	135	pF

The total load to be driven per phase is the sum of the capacitance of the phase to substrate plus the inter-phase capacitance to each of the adjacent phases. For the AØ1 and BØ1 phases the total is 26.6 nF, for the AØ2, AØ3, BØ2 and BØ3 phases the total is 14 nF and for all CØ phases the total is 355 pF.

POWER UP/POWER DOWN

When powering the device up or down, it is critical that any specified maximum rating is not exceeded. Specifically the voltage for the amplifier and dump drains must never be taken negative with respect to the substrate. Hence, since the substrate is to be operated at a positive voltage, then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero.

It is also important to ensure that excess currents (see notes 19 and 22) do not flow in the OS or DOS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

Similarly, for powering down, the substrate must be taken to zero voltage before the drains.

POWER CONSUMPTION

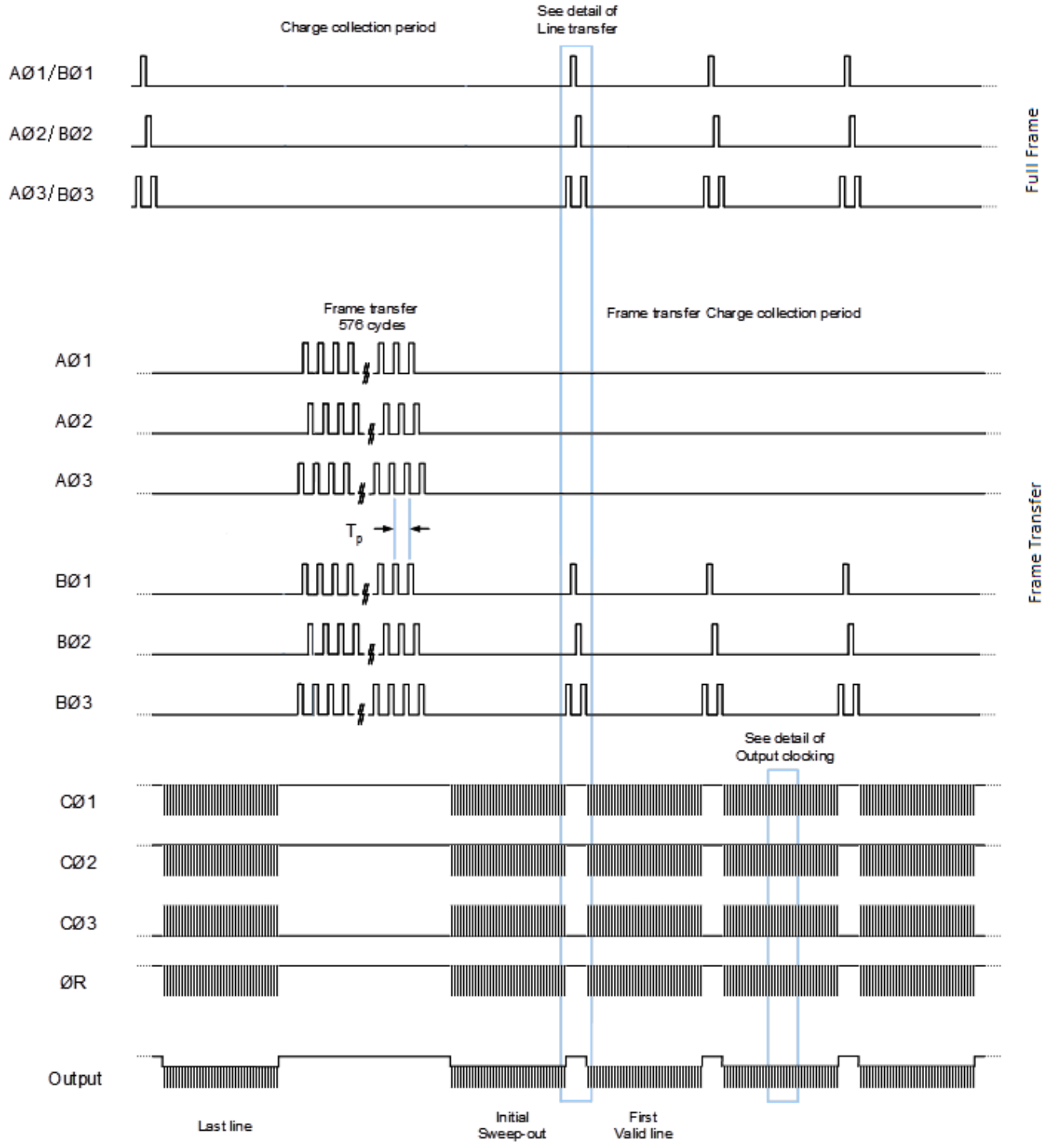
The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from the parallel and serial clocking (i.e. driving the capacitive loads).

The table below gives calculated values for the components of the power dissipation for different frame rates. The frequency is that for clocking the serial register. The clock period for parallel transfer is taken to be 20 µs (near the minimum).The amplifier power dissipation is the on-chip component for both A1 and A2. The clocked power dissipation is distributed between the device and the clock buffers.

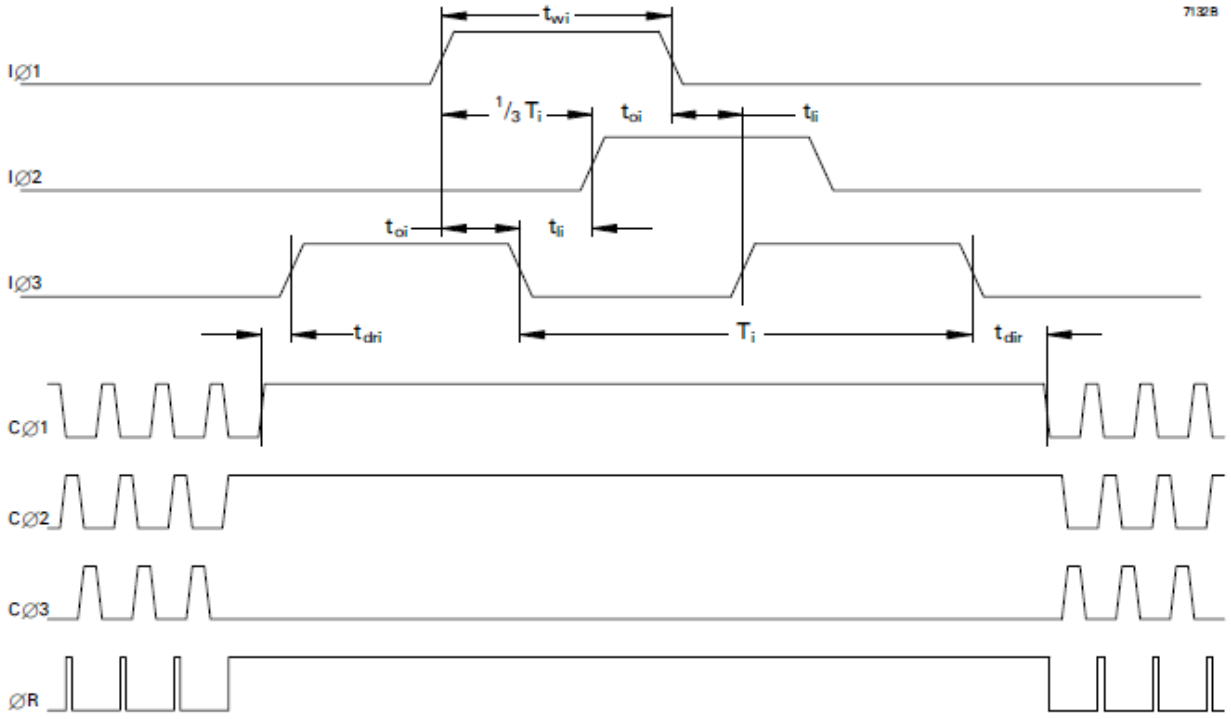
Read-out frequency	Frame time	Mean power dissipation			
		Amplifiers	Serial clocks	Parallel clocks	Total
100 kHz	7.2 s	130 mW	10 mW	1 mW	141 mW
1 MHz	742 ms	130 mW	105 mW	10 mW	245 mW
3 MHz	263 ms	130 mW	320 mW	30 mW	480 mW

The dissipation reduces to only that of the amplifiers during any time that charge is being collected in the image sections with both the parallel and serial clocks static.

TIMING DIAGRAM

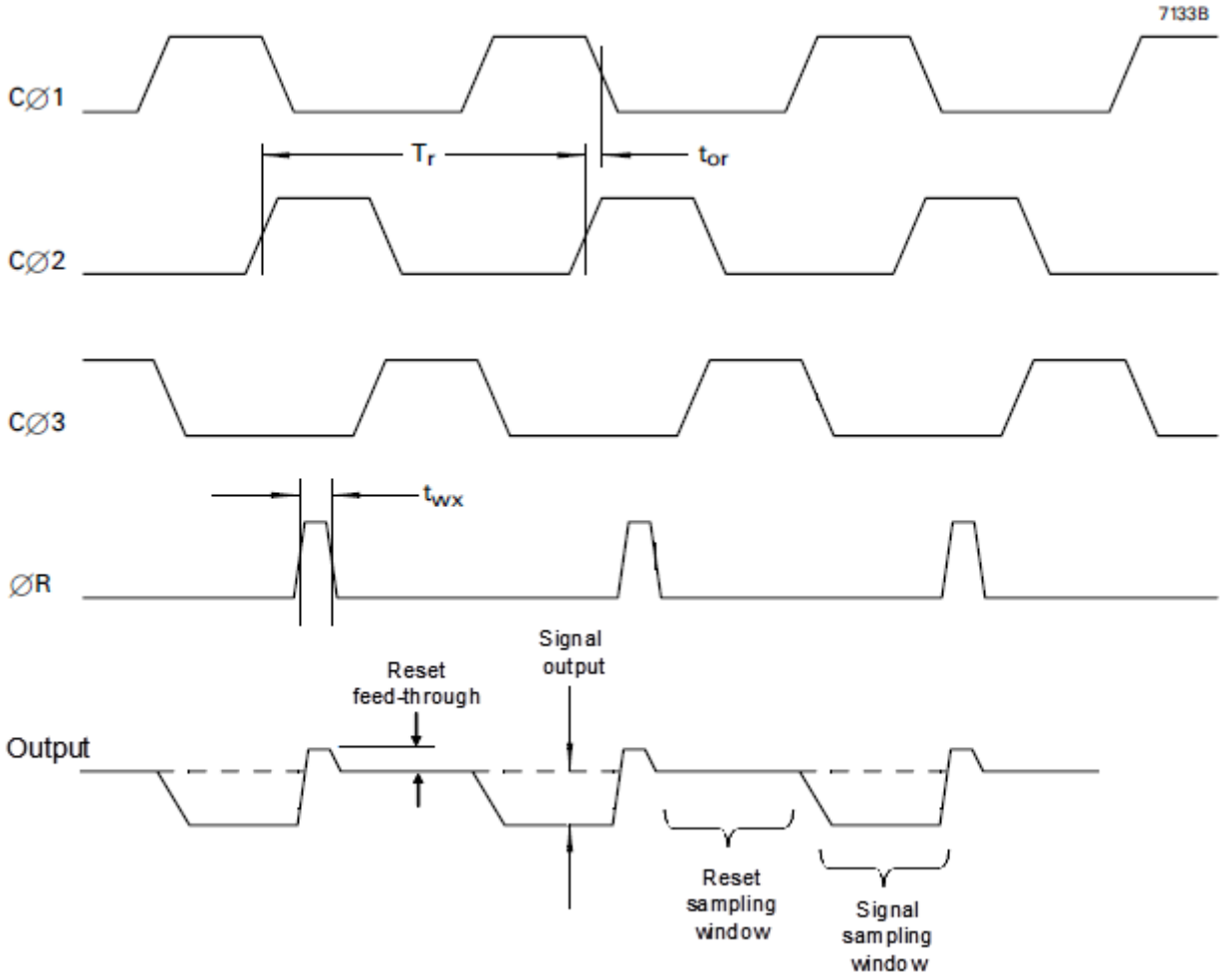


DETAIL OF LINE TRANSFER

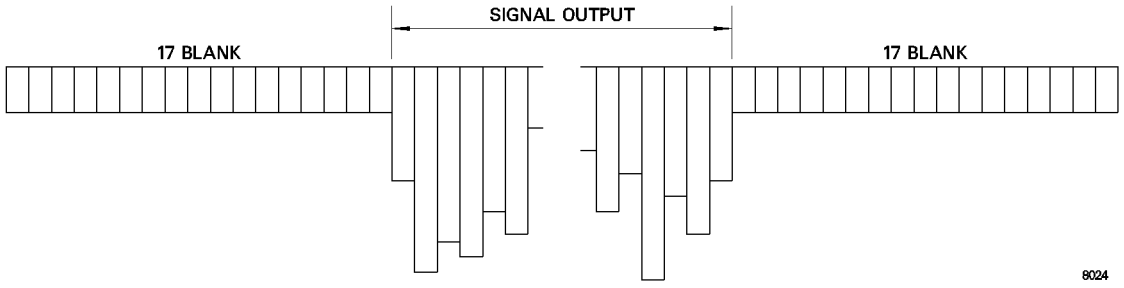


Note: For Full Frame readout, IØ = AØ = BØ. For Frame Transfer, IØ = BØ whilst AØ is low for charge collection.

DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



CLOCK TIMING REQUIREMENTS

The table below details some limitations on the clock timing. Where no value is shown, the timing is either not critical or will be defined by the required readout rate.

For AIMO operation, the first image electrode to be taken high after the all-low integrate phase should be Ø3 and the image clock period for this first phase after integration should be extended by at least 20µs compared to the standard image clock period T_i. The standard four pulse sequence, as shown in the detail of line transfer, is necessary to transfer a row to the register. For correct image row transfer, the voltage on the electrode should rise to at least 90% clock amplitude before the voltage on the previous phase electrode begins to fall. This in turn should reduce to below 10% clock pulse amplitude before the voltage on the next phase electrode begins to rise.

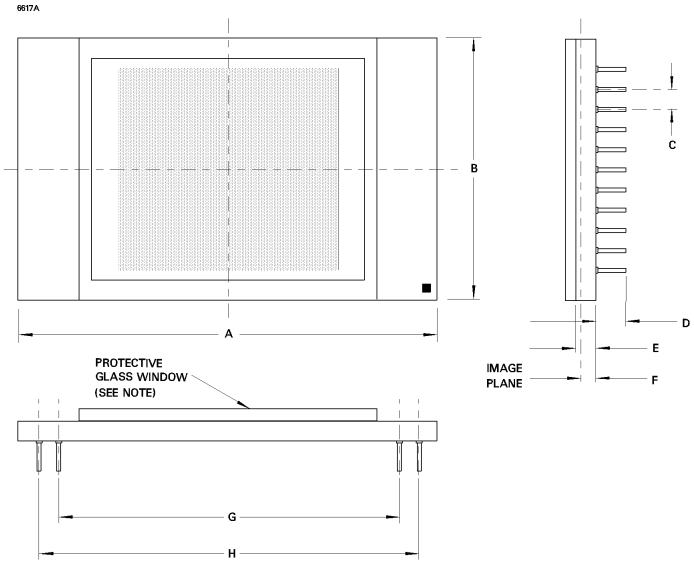
For the register section, CØ1 and CØ2 should be high to receive charge from the last image row. The order of clock pulses to CØ1 and CØ2 determine the direction of readout to either A1 or A2, with A2 shown above by default.

Symbol	Description	Min	Typ	Max	Unit
T_i	Image clock period	15	$3t_{op} + 3t_{ip}$	-	µs
T_{fi}	First Image clock period after integration	35	T_i +20		µs
t_{wi}	Image clock pulse width	8	$2t_{op} + 1t_{ip}$	-	
t_{ri}	Image clock pulse rise time (10 to 90%)	0.5	-	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	0.5	-	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	3	-	-	µs
t_{li}	Image clock pulse, two phase low	2	-	-	µs
t_{dir}	Delay time, BØ stop to CØ start	3	-	-	µs
t_{dri}	Delay time, CØ stop to BØ start	1	-	-	µs
T_r	Register clock period (note 23)	150	-	-	ns
t_{rr}	Register pulse rise time (at 10-90% levels)	10	-	$0.3T_r$	ns
t_{fr}	Register pulse fall time (at 90-10% levels)	10	-	$0.3T_r$	ns
t_{or}	Register pulse overlap	10	-	-	ns
t_{wx}	Reset pulse width (at 50% levels)	20	-	-	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	10	-	-	ns

NOTE

23 With the device pinned, the register clock overlaps required limit the maximum readout frequency to ~6 MHz for maximum charge signal transfer, but faster operation could be possible for some loss in peak signal. At readout frequencies below the maximum it can be advantageous to use an asymmetrical timing, where, the CØ2 pulse can be minimised to only the width required to contain the reset pulse thereby maximising the reset and signal sampling windows.

PACKAGE DETAIL



Outline Note

The device is normally supplied with a temporary glass window for protection purposes. It can also be supplied with a quartz or fibre-optic window where required.

Dimension	Distance (mm)	Tolerances
A	53.34	~ 1 %
B	33.00	~ 1 %
C	2.54	-
D	3.81	-
E	2.3	~ 10 %
F	<1.8	~ 10 %
G	43.18	~ 1 %
H	48.26	~ 1 %

The dimensions are provided for information.

"**E**" is the thickness of the package at the greatest point where the temporary window sits on an outer ledge.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be positively grounded

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (i.e. all CCD pins except SS, DD, RD, OD and OS) but not to the other pins.

The devices are assembled in a clean room environment. Teledyne e2v technologies recommend that similar precautions are taken to avoid contaminating the active surface.

PART REFERENCES

For ordering information, some existing part numbers are below. Contact Teledyne e2v for other variants.

CCD55-30-*-xxx
* = cosmetic grade
xxx = device specific part number

Part Number	Description
CCD55-30-*-348	Full Frame, Basic Midband, No Window
CCD55-30-*-359	Full Frame, Basic Uncoated, No Window
CCD55-30-*-S17	Full Frame, Basic Broadband, No Window

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to ionising radiation. Characterisation data is held at Teledyne e2v technologies with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

TEMPERATURE RANGE

Operating temperature range 153 - 323 K

Storage temperature range 143 - 358 K

Operation or storage in humid conditions may give rise to ice on the surface when the sensor taken to low ambient temperatures, thereby causing irreversible damage.

Maximum rate of heating or cooling: 5 K/min.