e2v technologies

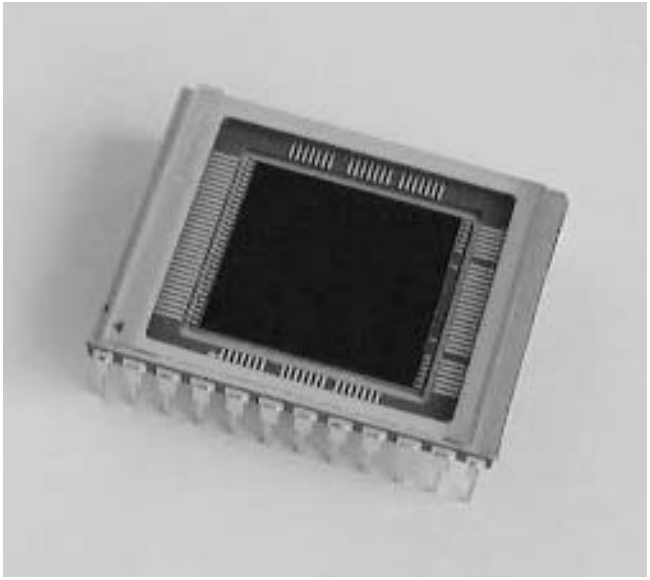
CCD77-00 Front Illuminated High Performance IMO Device

FEATURES

- 512 by 512 Image Format
- Image Area 12.3 x 12.3 mm
- Full-Frame Operation
- 24 μm Square Pixels
- Low Noise Output Amplifiers
- 100% Active Area
- Inverted Mode Operation

APPLICATIONS

- Spectroscopy
- Scientific Imaging
- Star Tracking
- Medical Imaging



INTRODUCTION

The CCD77 family of sensors are full-frame devices with readout registers above and below the image section. The top register, image section and bottom register are designated A, B and C respectively. Each register has a single output at one end and a charge injection structure at the other end for test purposes.

Standard three-phase clocking and buried channel charge transfer are employed. The image section of the device operates in inverted mode for minimum dark current. To maximise the dynamic range, the CCD is manufactured without anti-blooming structures.

In common with other e2v technologies CCD Sensors, the front illuminated CCD77-00 is available with a fibre-optic window or taper.

Designers are advised to consult e2v technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging.

TYPICAL PERFORMANCE

Maximum readout frequency	7	MHz
Output responsivity	2.5	$\mu V/e^-$
Peak signal	300	ke^-/pixel
Dynamic range (at 20 kHz)	~100 000:1	
Spectral range	400 - 1060	nm
Readout noise (at 20 kHz)	3.0	e^- rms

GENERAL DATA

Format

Image area	12.3 x 12.3	mm
Active pixels (H)	512	
(V)	512	
Pixel size	24 x 24	μm
Number of output amplifiers	2	

15 additional pixels are provided for over-scanning purposes in each register.

Package

Package size	22.6 x 29.9	mm
Number of pins	24	
Inter-pin spacing	2.54	mm
Inter-row spacing	22.86	mm
Window material	quartz or removable glass	
Type	ceramic DIL array	
Weight (approx, no window)	6	g

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PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	300k	350k	-	e^-/pixel
Peak output voltage (no binning)	-	875	-	mV
Dark signal at 293 K (see notes 2 and 3)	-	200	400	e^-/pixel/s
Dynamic range (see note 4)	-	100 000:1	-	
Charge transfer efficiency (see note 5): parallel serial	 - -	 99.9999 99.9993	 - -	 % %
Output amplifier responsivity (see note 3)	1.8	2.5	3.5	$\mu V/e^-$
Readout noise at 253 K (see notes 3 and 6)	-	3.0	5.0	rms e^-/pixel
Maximum readout frequency (see note 7)	-	1000	7000	kHz
Dark signal non-uniformity at 293 K (std. deviation) (see notes 3 and 8)	-	80	160	e^-/pixel/s
Response non-uniformity (std. deviation)	-	1	3	% of mean
Output node capacity	-	600k	-	electrons

NOTES

1. Signal level at which resolution begins to degrade.
2. Measured between 253 and 293 K and V_{SS} +9.5 V typically. Dark signal at any temperature T (kelvin) may be estimated from:

   $$Q_d/Q_{d0} = 1.14 \times 10^6 T^3 e^{-9080/T}$$

   where Q_{d0} is the dark signal at T = 293 K (20 °C).
3. Test carried out at e2v technologies on all sensors.
4. Dynamic range is the ratio of full-well capacity to readout noise measured at 253 K and 20 kHz readout speed.
5. CCD characterisation measurements made using charge generated by X-ray photons of known energy.
6. Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 20 µs integration period.
7. Readout at speeds in excess of 7 MHz can be achieved but performance to the parameters given cannot be guaranteed.
8. Measured between 253 and 293 K, excluding white defects.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 253 K.

Slipped columns Are counted if they have an amplitude greater than 200 e^-.

Black spots Are counted when they have a signal level of less than 90% of the local mean at a signal level of approximately half full-well.

White spots Are counted when they have a generation rate 50 times the specified maximum dark signal generation rate (measured between 253 and 293 K). The typical temperature dependence of white spot defects is different from that of the average dark signal and is given by:

$$Q_d/Q_{d0} = 122T^3 e^{-6400/T}$$

White column A column which contains at least 9 white defects.

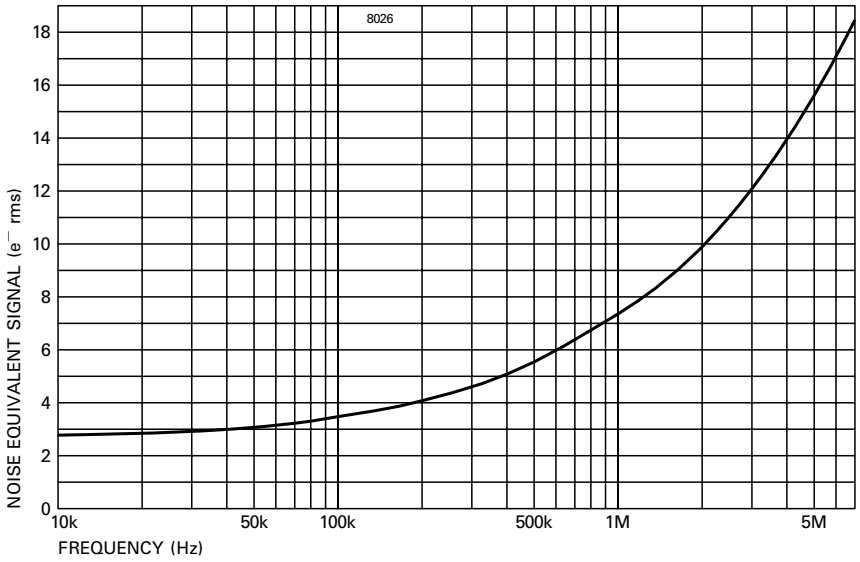
Black column A column which contains at least 9 black defects.

GRADE	0	1	2
Column defects: black or slipped white	 0 0	 1 0	 6 0
Traps >200 e^-	1	2	6
White spots	10	15	50
Black spots	10	15	30

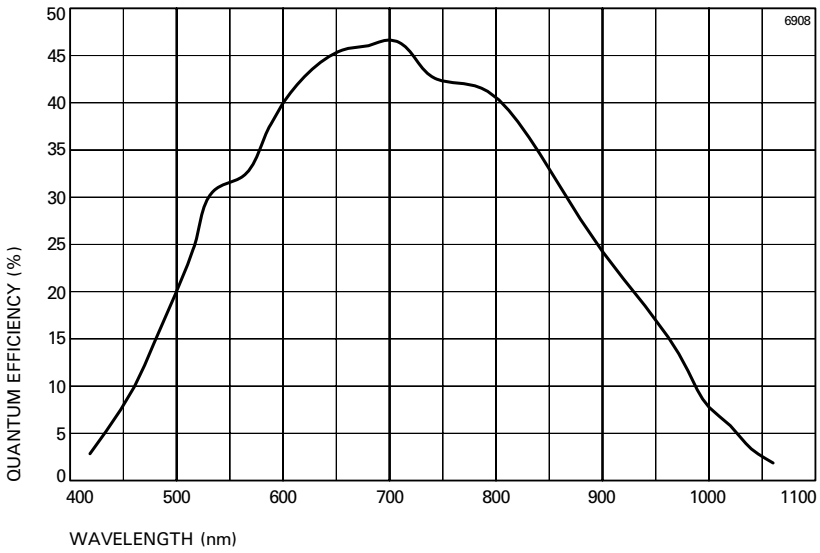
Grade 5 Devices which are fully functioning, with image quality below that of grade 2, and which may not meet all other performance parameters.

Note The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 253 K. The amplitude of white spots and columns will decrease rapidly with temperature.

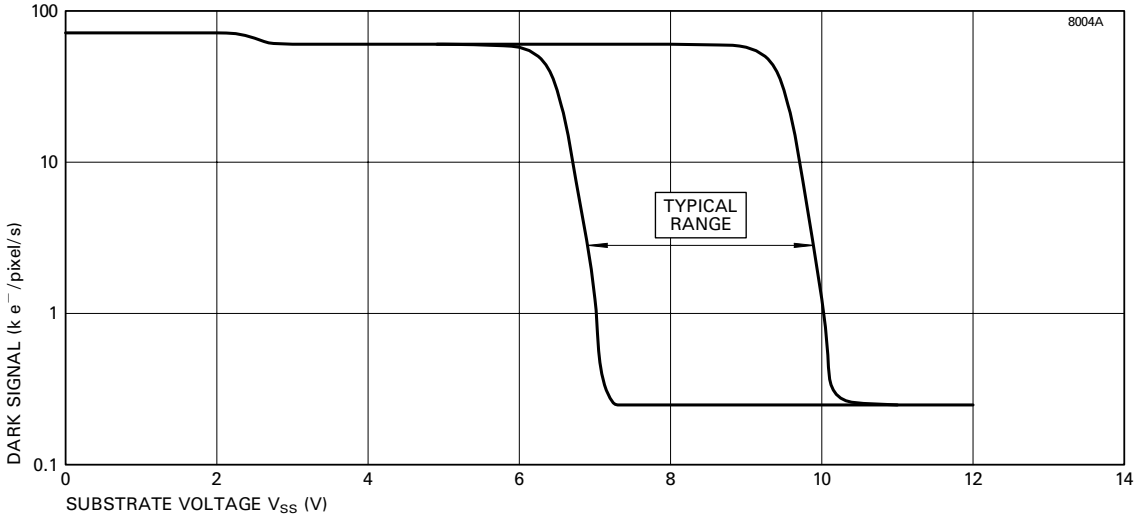
TYPICAL OUTPUT CIRCUIT NOISE



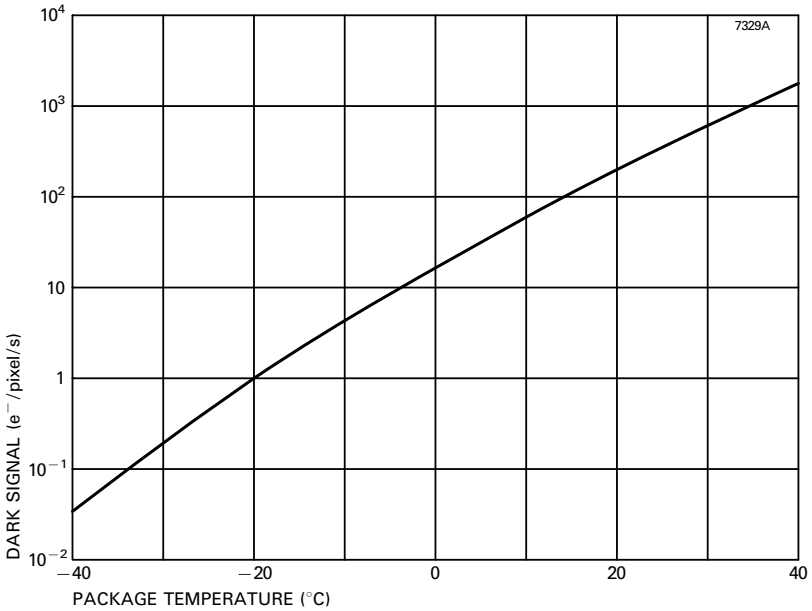
TYPICAL SPECTRAL RESPONSE



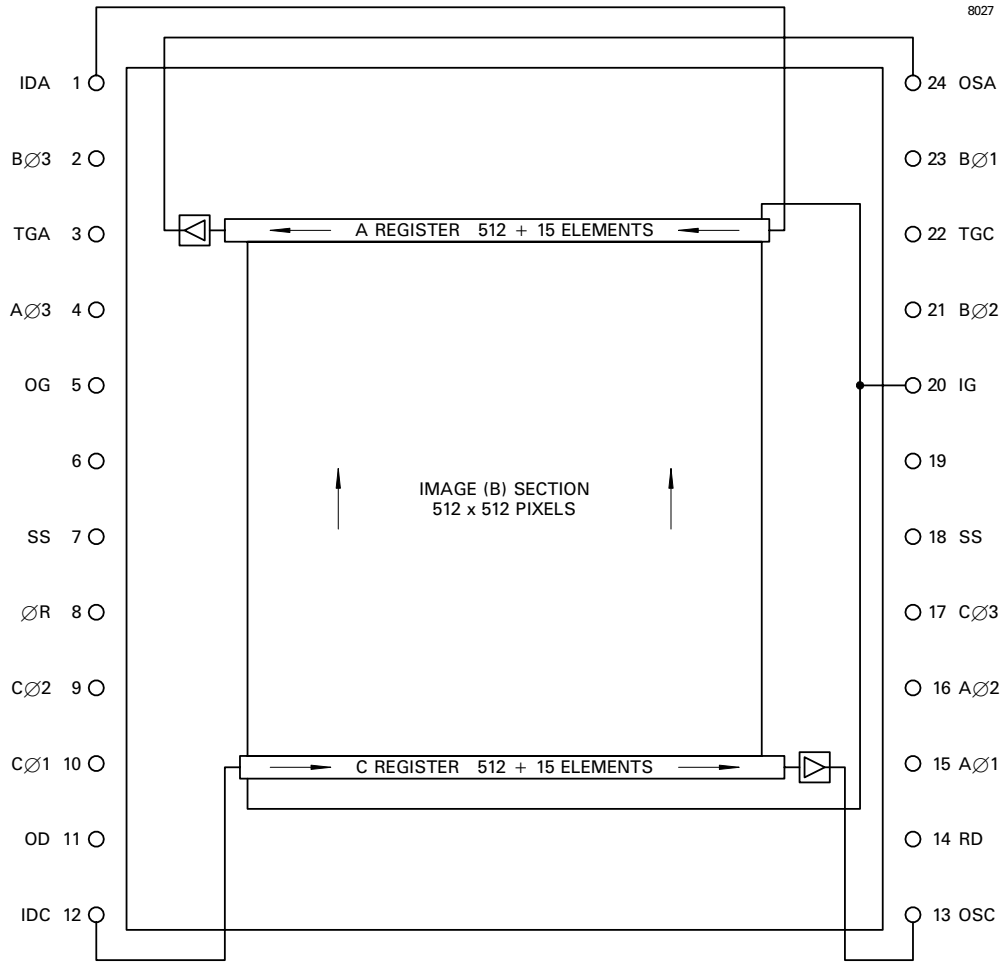
TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE (V_{SS} = +9.5 V)



DEVICE SCHEMATIC



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	CLOCK LOW TYPICAL	PULSE AMPLITUDE OR DC LEVEL (V)			MAXIMUM RATINGS with respect to V_{SS}
				Min	Typical	Max	
1	IDA	Input diode A	0	see note 9			±20 V
2	B∅3	Image clock	0	10	12	15	±20 V
3	TGA	Transfer gate A	0	10	12	15	±20 V
4	A∅3	Register clock A	1	8	10	15	±20 V
5	OG	Output gate (A and C)	n/a	1	3	5	±20 V
6	-	No connection	0	-			-
7	SS	Substrate	n/a	8	9.5	11	-
8	∅R	Reset (A and C)	0	8	12	15	±20 V
9	C∅2	Register clock C	1	8	10	15	±20 V
10	C∅1	Register clock C	1	8	10	15	±20 V
11	OD	Output drain (A and C)	0	27	29	32	−0.3 to +35 V
12	IDC	Input diode C	0	see note 9			±20 V
13	OSC	Output source C	0	see note 10			−0.3 to +25 V
14	RD	Reset drain (A and C)	0	15	17	19	−0.3 to +25 V
15	A∅1	Register clock A	1	8	10	15	±20 V
16	A∅2	Register clock A	1	8	10	15	±20 V
17	C∅3	Register clock C	1	8	10	15	±20 V
18	SS	Substrate	0	8	9.5	11	-
19	-	No connection	0	-			-
20	IG	Input gate	0	8	10	15	±20 V
21	B∅2	Image clock	0	10	12	15	±20 V
22	TGC	Transfer gate C	0	10	12	15	±20 V
23	B∅1	Image clock	0	10	12	15	±20 V
24	OSA	Output source A	0	see note 10			±20 V

Maximum voltages between pairs of pins:
- pin 11 (OD) to pin 24 (OSA) . . . . . ±15 V
- pin 11 (OD) to pin 13 (OSC) . . . . . ±15 V

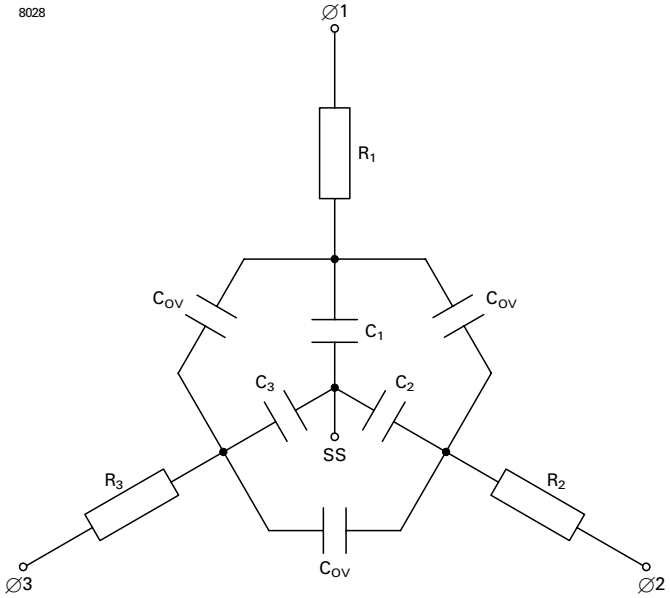
Maximum output transistor current . . . . . 10 mA

NOTES

9. For normal operation, the input gate should be set to 0 V and the input diode to approx. 22 V. To inject charge for test purposes, the input gate should be pulsed high during the period when A∅1 is high and the input diode should be adjusted for the required charge injection. Typical uses for such charge injection include assessing charge transfer efficiency, and the measurement of output responsivity using the reset drain current method.
10. 3 to 5 V below OD. Connect to ground using a 5 mA current source or appropriate load resistor (typically 5 kΩ).
11. All devices will operate at the typical values given. However, some adjustment within the minimum to maximum range may be required to optimise performance for critical applications. It should be noted that conditions for optimum performance may differ from device to device.
12. With the B∅ connections shown, charge is transferred to the top register, A. In order to transfer charge to the bottom register, B∅1 and B∅2 connections should be reversed. Refer to the waveform diagram.

ELECTRICAL INTERFACE CHARACTERISTICS

An approximate equivalent circuit to represent the load presented by the image section or output registers is shown below.



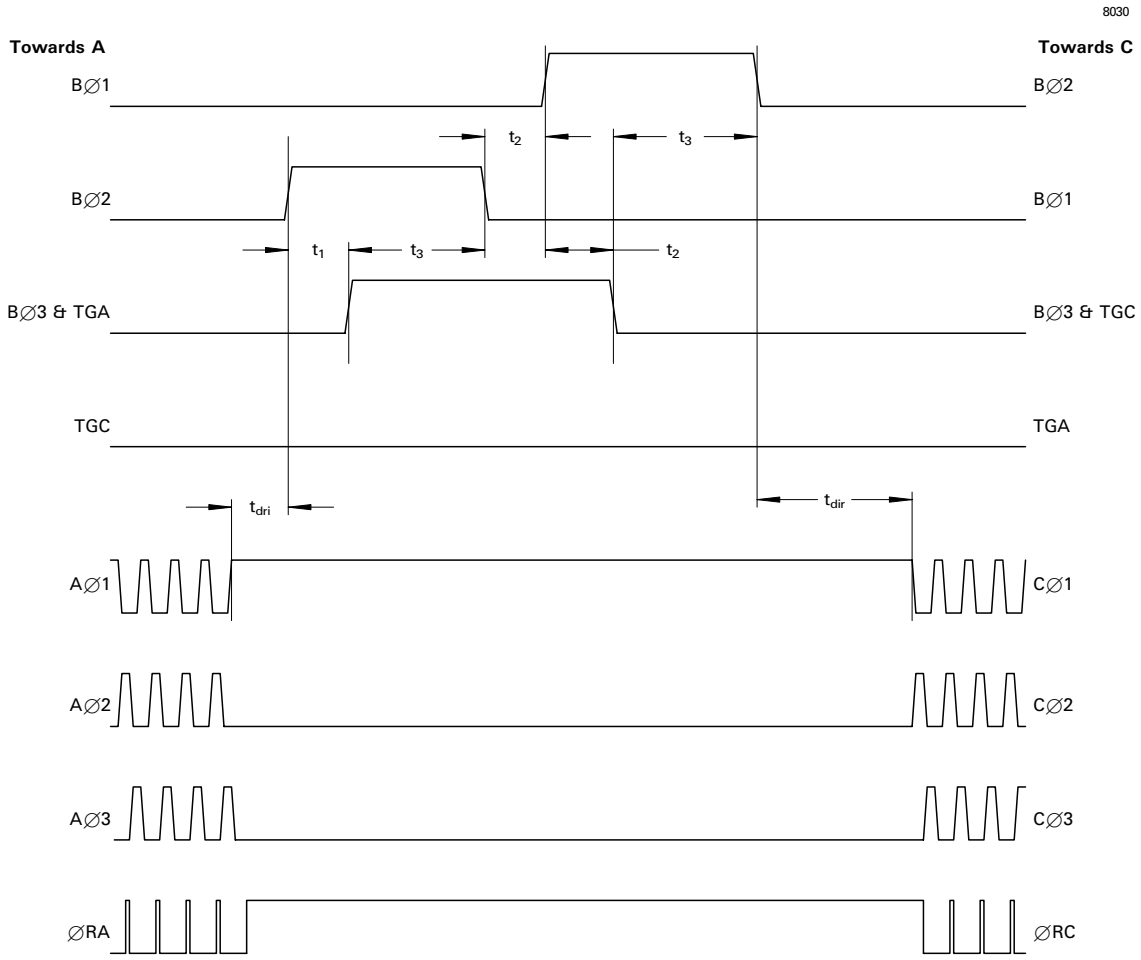
Typical Electrode Capacitances (measured at mid-clock level)

I∅/I∅ interphase (C_{OV})	1.6	nF
I∅1/SS and I∅2/SS (C_1, C_2)	3.5	nF
I∅3/SS (C_3)	12	nF
R∅/R∅ interphase	30	pF
R∅/SS	60	pF
∅R/SS	20	pF

Typical Electrode Series Resistance

I∅1 and I∅2 (R_1, R_2)	20	Ω
I∅3 (R_3)	14	Ω
R∅1, 2, 3	20	Ω
Output amplifier impedance at typical operating conditions	400	Ω

DETAIL OF LINE TRANSFER



Clocking Sequence

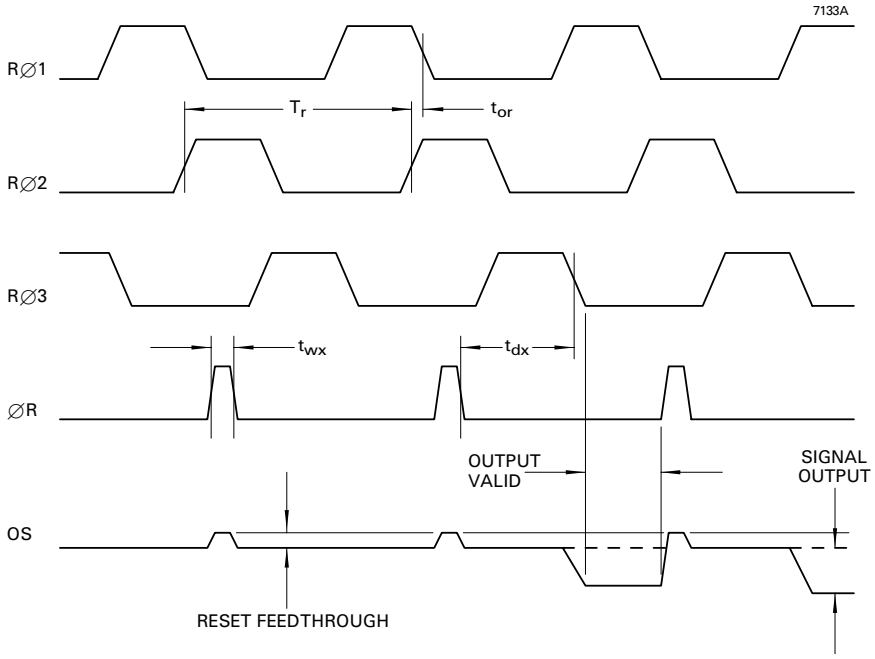
During the integration period, all BØ electrodes should be low – the IMO implant takes care of charge gathering.

For transfer to the A register, use the labelling of waveforms on the left of the diagram. Charge is transferred to the register when BØ3 and TGA are taken from high to low.

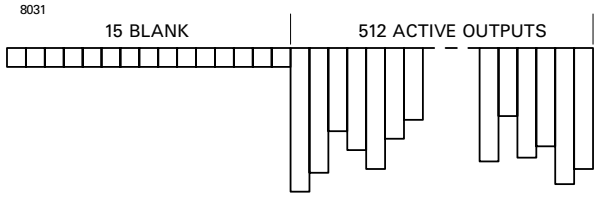
For transfer to the C register, use the labelling of waveforms on the right of the diagram. Charge is transferred to the register when BØ3 and TGC are taken from high to low.

If only one register is used, the recommended approach for the unused register is to tie its clocks high and its TG low. Any charge collected in the unused register would then spill over OG and drain out through RD, thus keeping unwanted charge out of the image section. Continuous clocking of the unused register can be used but may generate extra heat, potentially causing more dark current in the image area.

DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



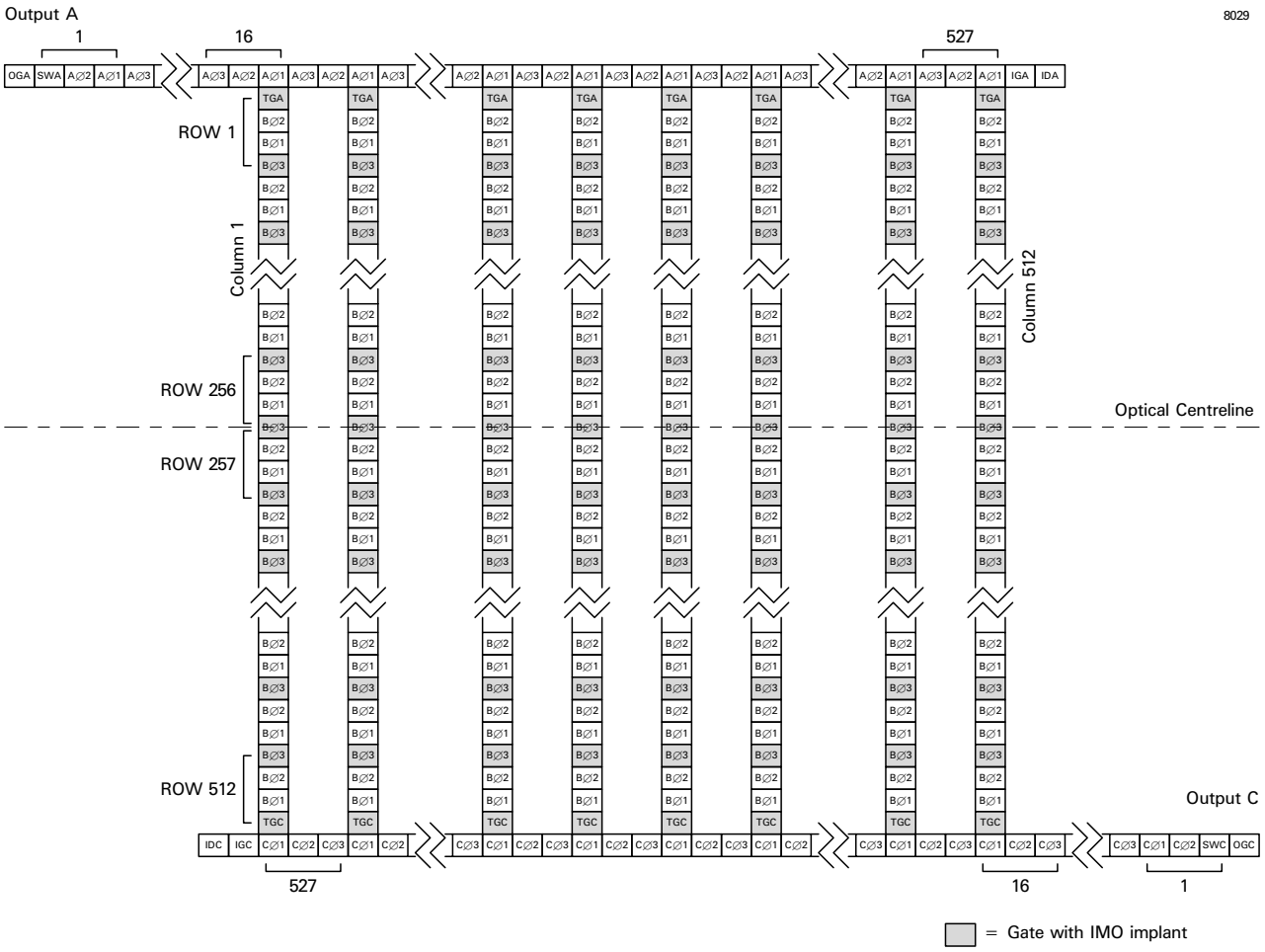
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
t_1	Image clock overlap/delay	0.65	1.0	see note 13	µs
t_2	Image clock overlap/delay	0.65	1.0	see note 13	µs
t_3	Image clock overlap/delay	1.1	2.0	see note 13	µs
t_{dri}	Post register clocking delay	1.0	2.0	see note 13	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.1	5	$T_i - 2t_{wi}$	µs
t_{dir}	Pre register clocking delay	1.65	3.0	see note 13	µs
t_{ltr}	Line transfer/vertical shift time	7.0	14.0	see note 13	µs
T_r	Output register clock cycle period	140	1000	see note 14	ns
t_{rr}	Clock pulse rise time (10 to 90%)	20	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	10	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	20	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	$0.2t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

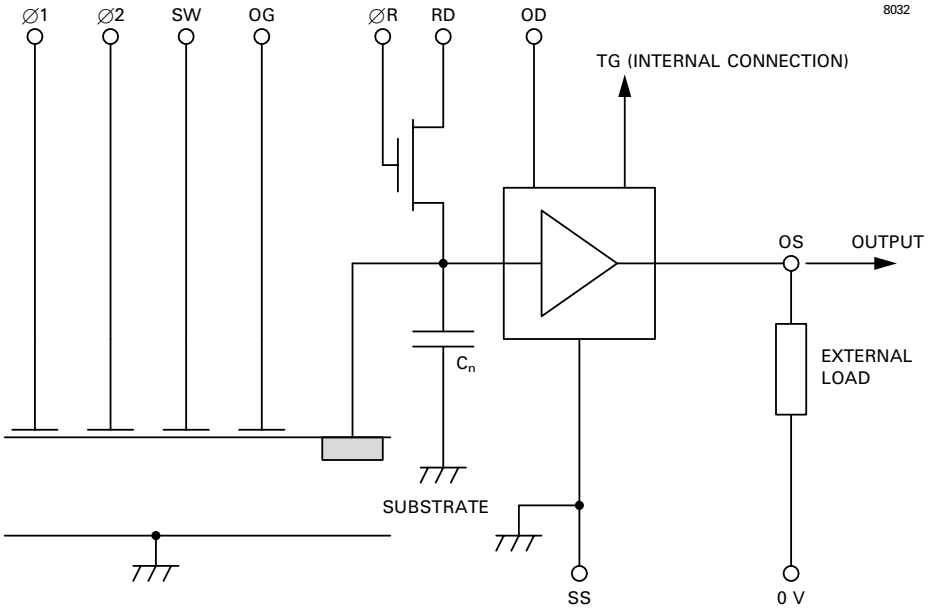
NOTES

13. No maximum other than that set by system constraints on the total readout period.
14. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.

FUNCTIONAL DIAGRAM



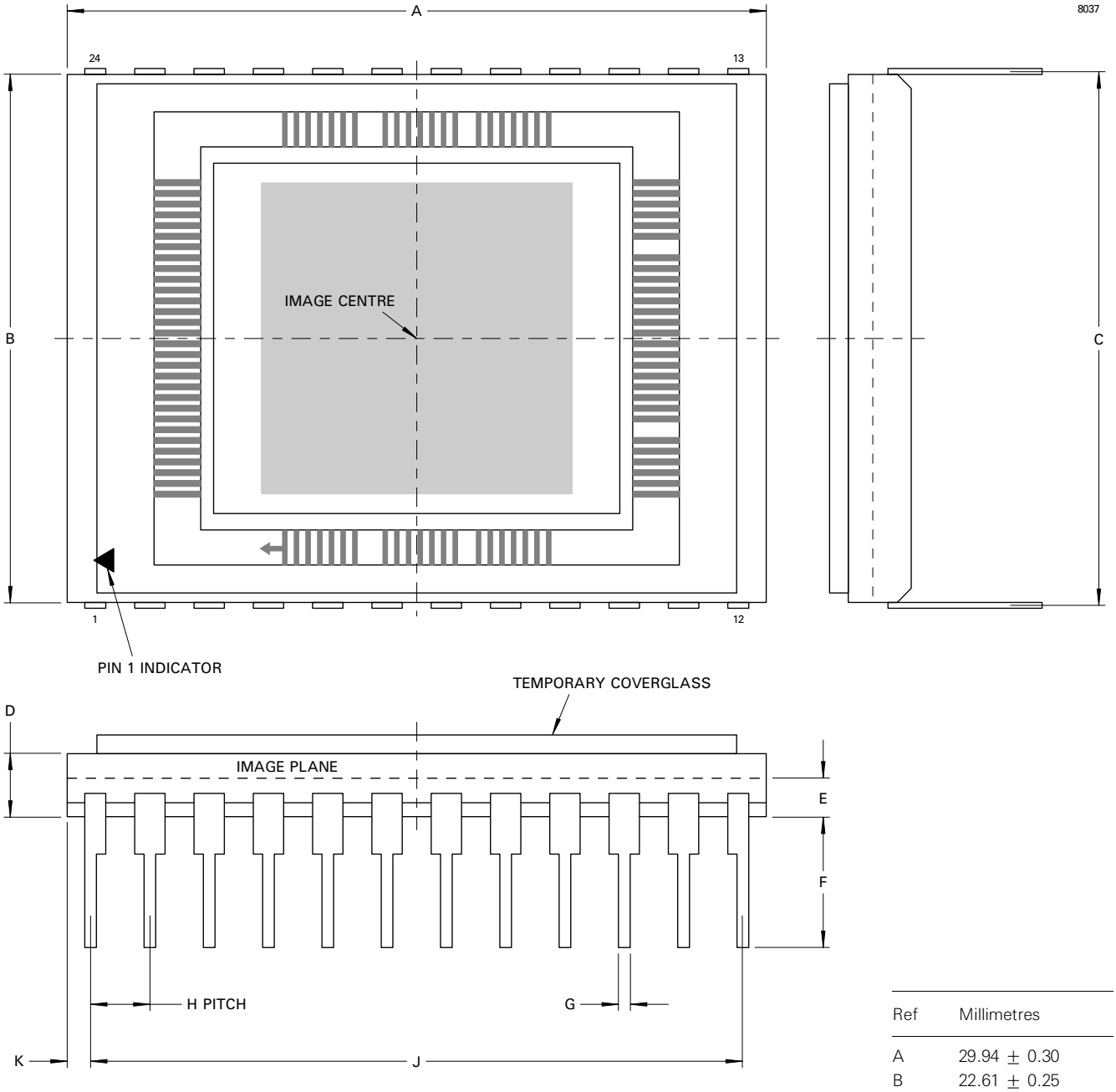
OUTPUT CIRCUIT



NOTE

15. SW will be joined to ∅3 in the proposed package.

OUTLINE
(All dimensions without limits are nominal)



Ref	Millimetres
A	29.94 ± 0.30
B	22.61 ± 0.25
C	22.86 ± 0.25
D	2.70 ± 0.27
E	1.65 ± 0.25
F	5.6 ± 0.5
G	0.46 ± 0.05
H	2.54 ± 0.13
J	27.94 ± 0.13
K	1.0 ± 0.3

ORDERING INFORMATION

Options include:

- Temporary Glass Window
- Permanent Window; ask for details
- Fibre-optic Coupling
- UV Coating
- X-ray Phosphor Coating

For further information on the performance of these and other options, please contact e2v technologies.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty.

HIGH ENERGY RADIATION

Device characteristics will change when subject to ionising radiation.

Users planning to operate CCDs in high radiation environments are advised to contact e2v technologies.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	153	–	373	K
Operating	153	273	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling . . . . 5 K/min